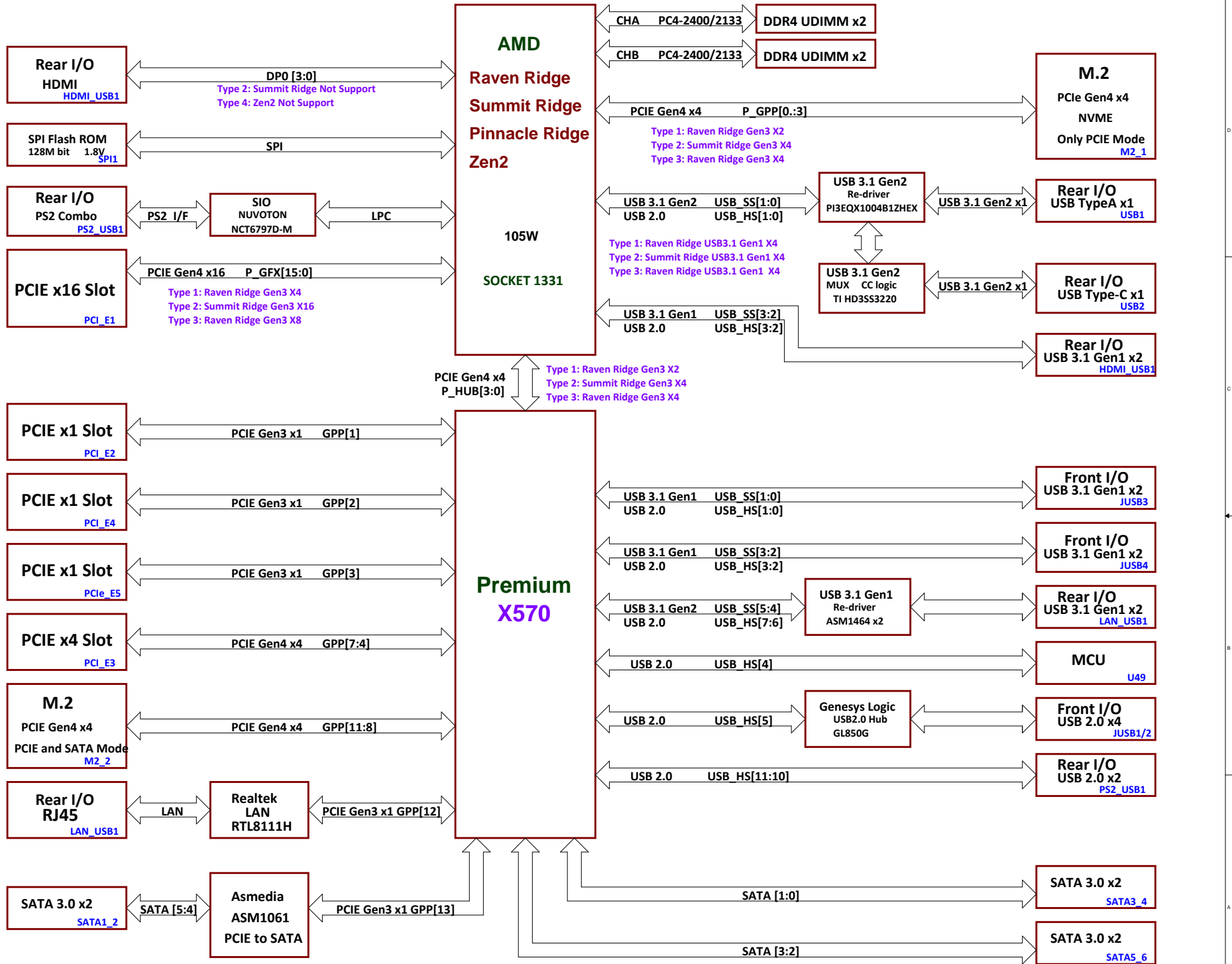
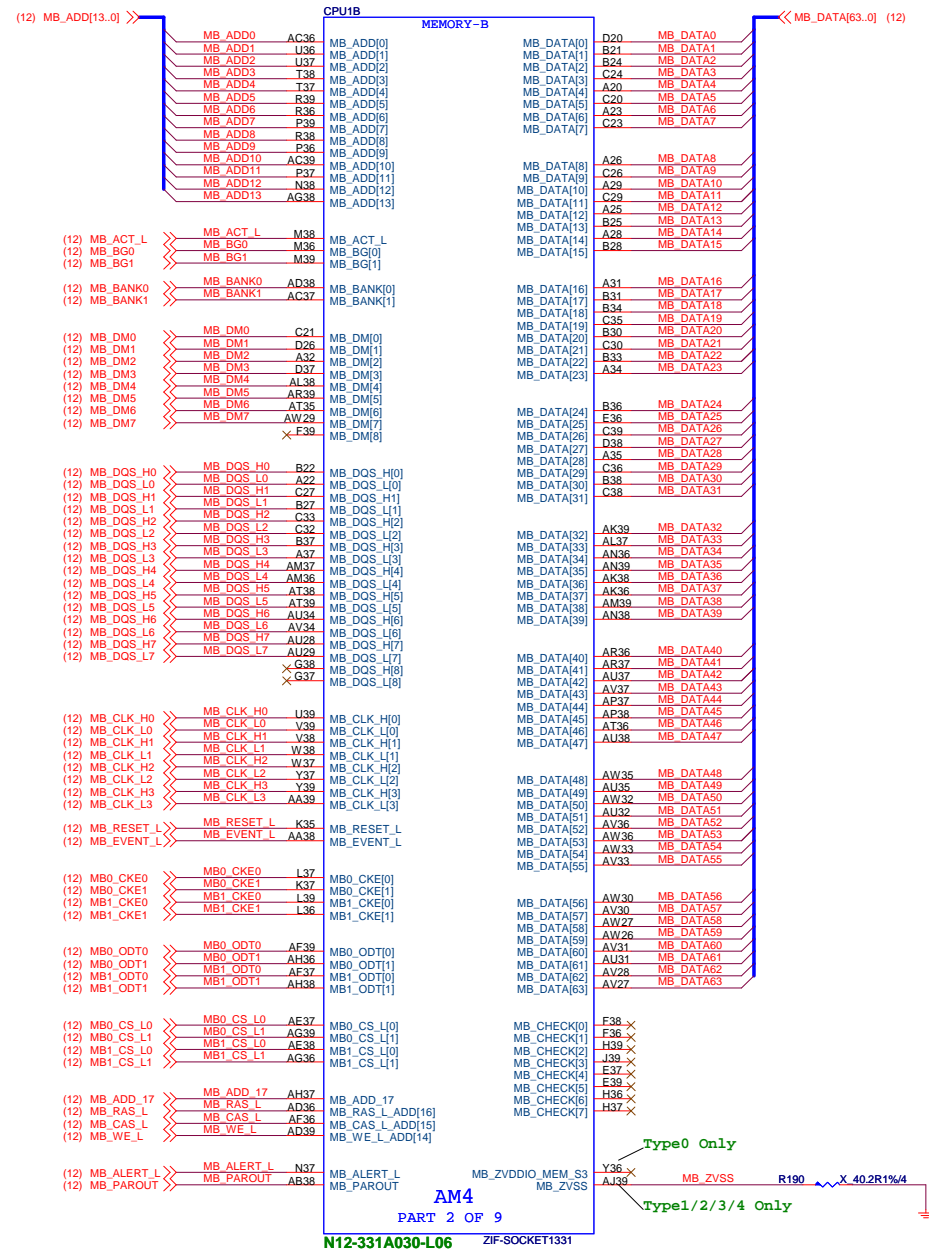
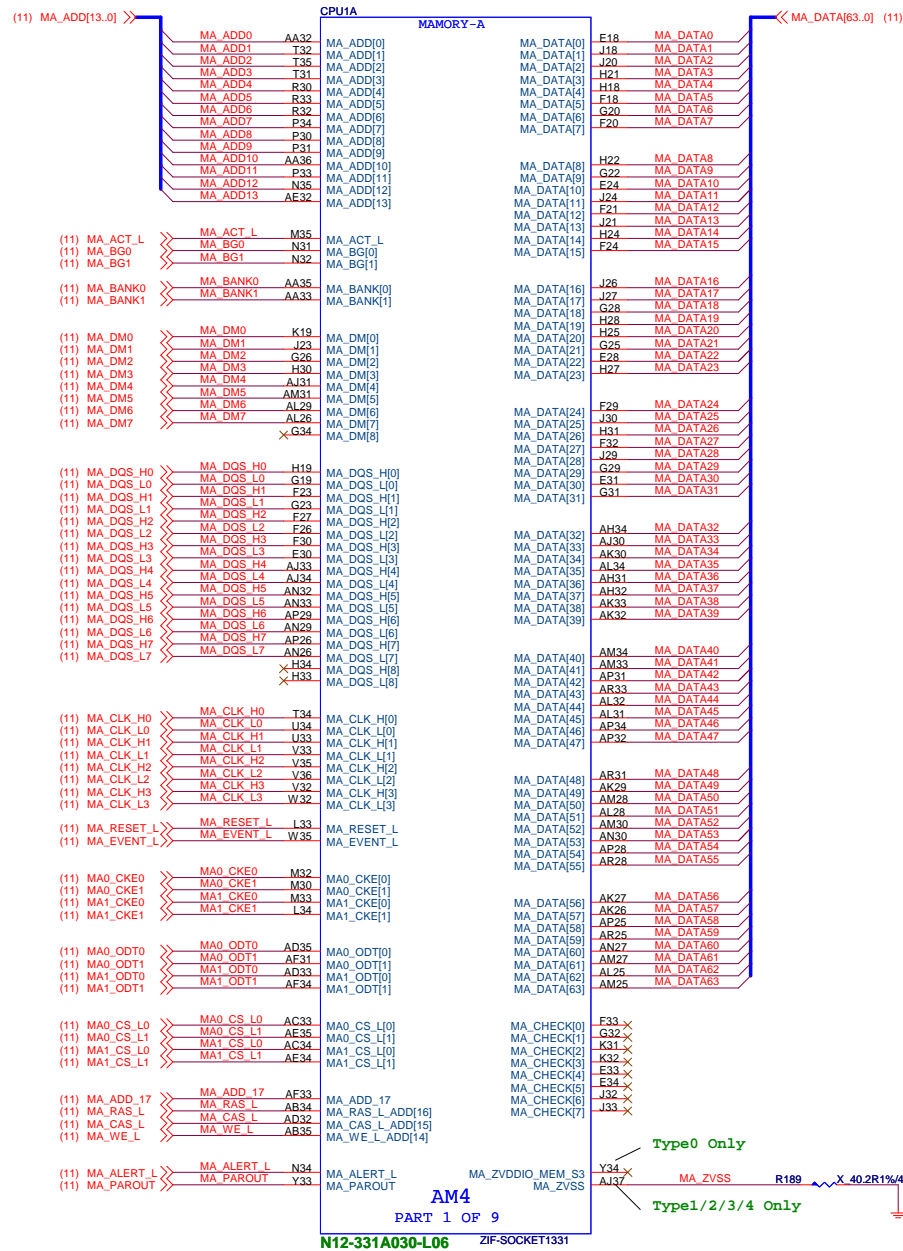


# AMD AM4

## GAMING EDGE AC

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02	Block Diagram	37	Audio ALC1220P-VB	67	LED - Power / JPIPE
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35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		





MICRO-STAR INT'L CO.,LTD

MS-7C37

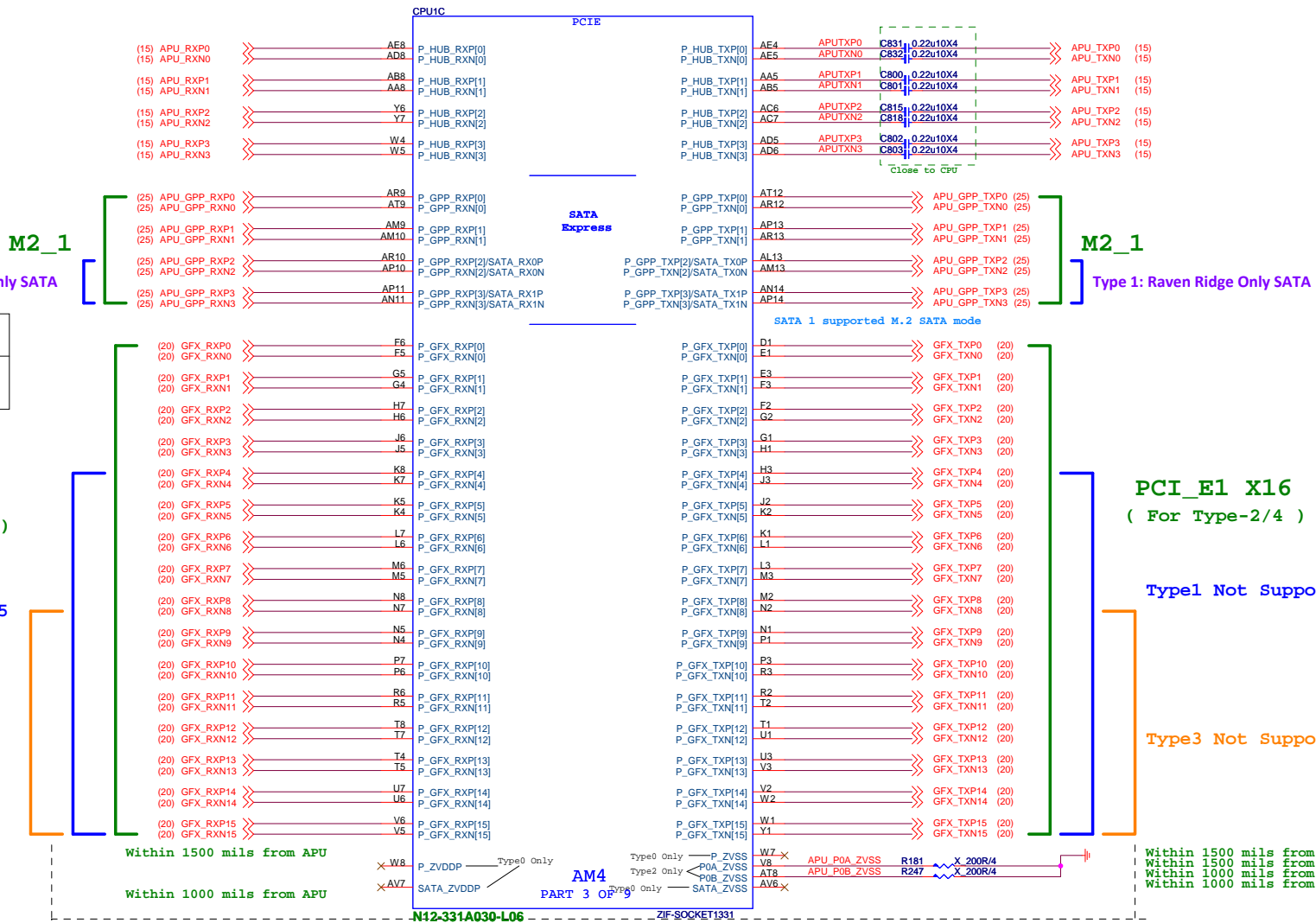
Size	Document Description	Rev
Custom	AM4 DDR4 I/F	3.0
Date: Friday, April 12, 2019		
Sheet 3 of 75		

TYPE	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

PCI\_E1 X16  
( For Type-2/4 )

Type1 Not Supported GFX 4~15

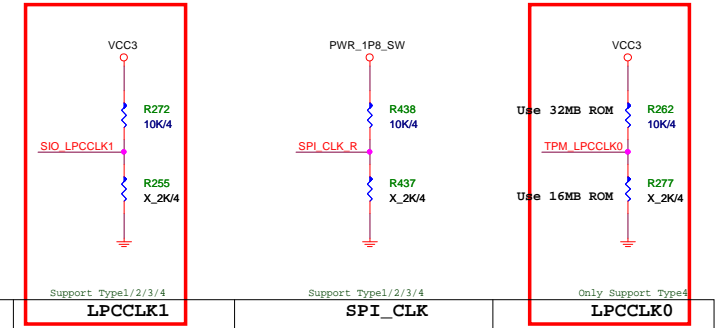
Type3 Not Support GFX 8~15



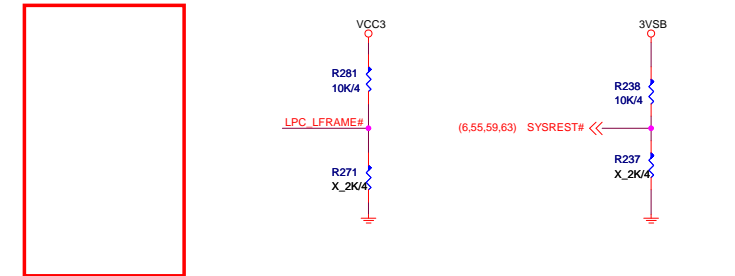




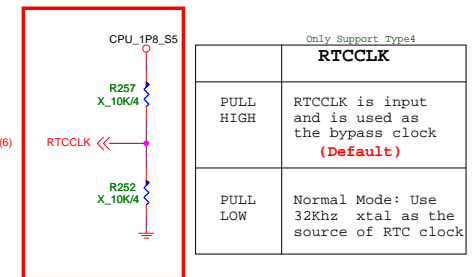
# Strapping Options



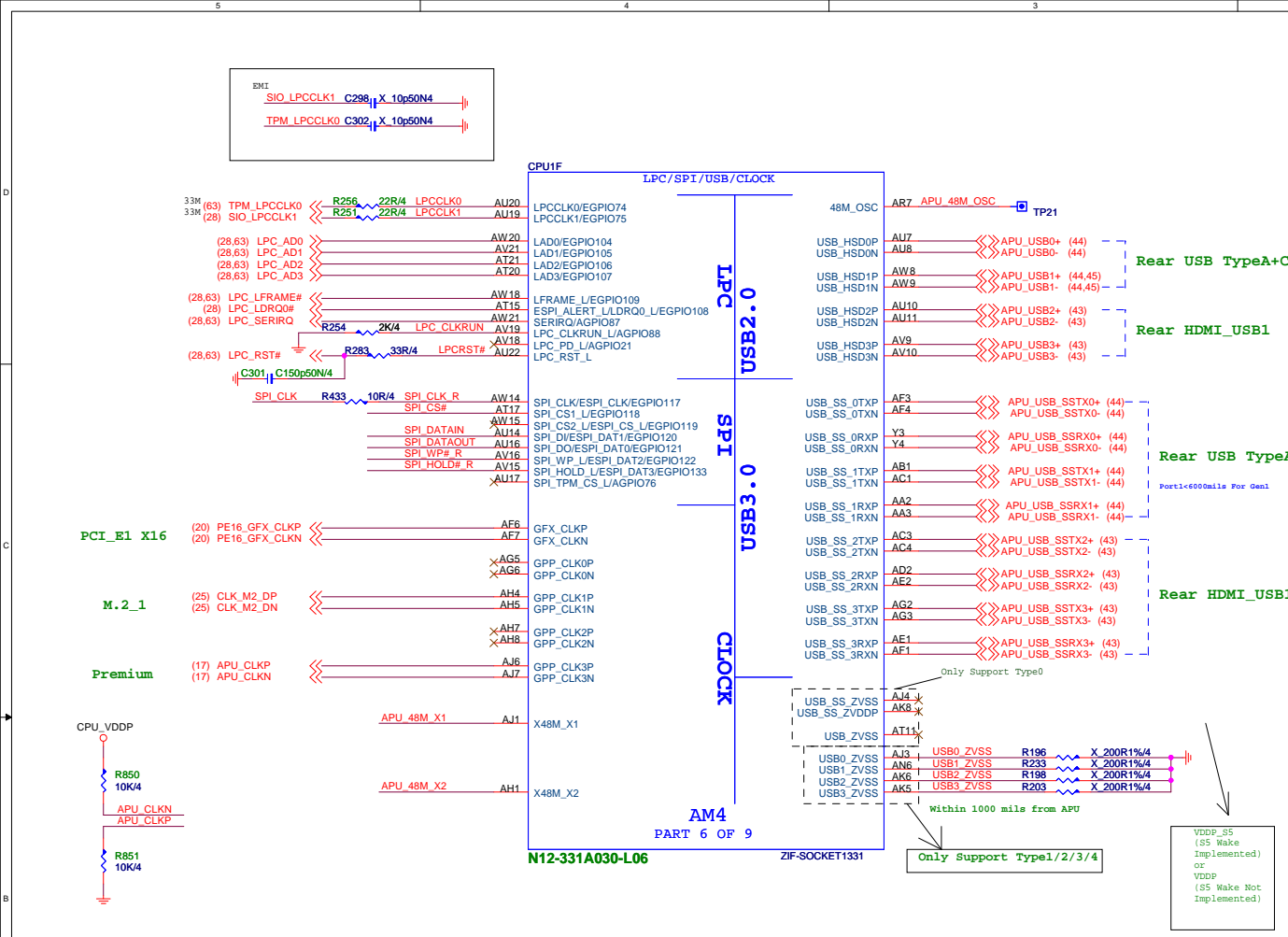
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



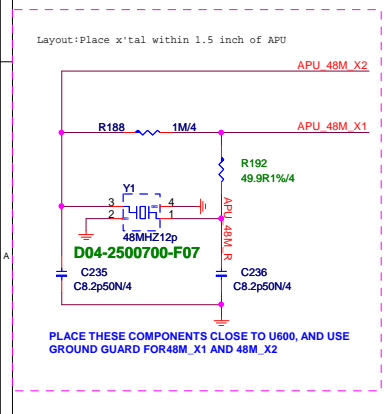
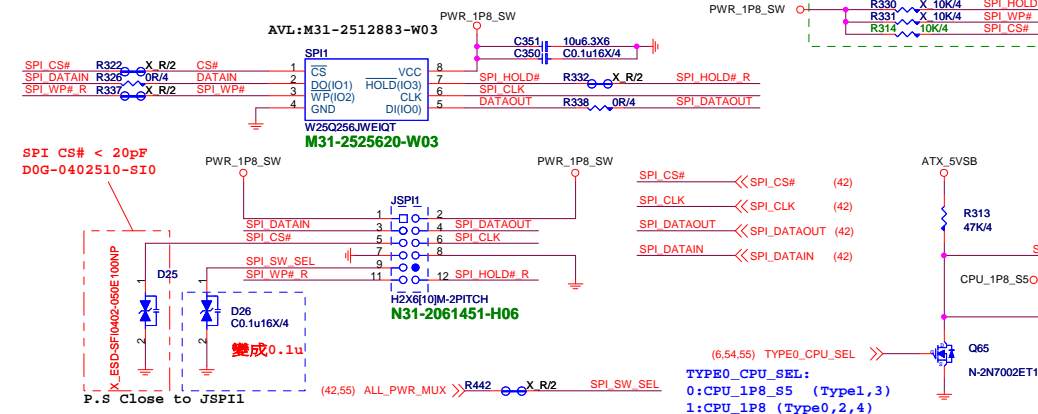
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode



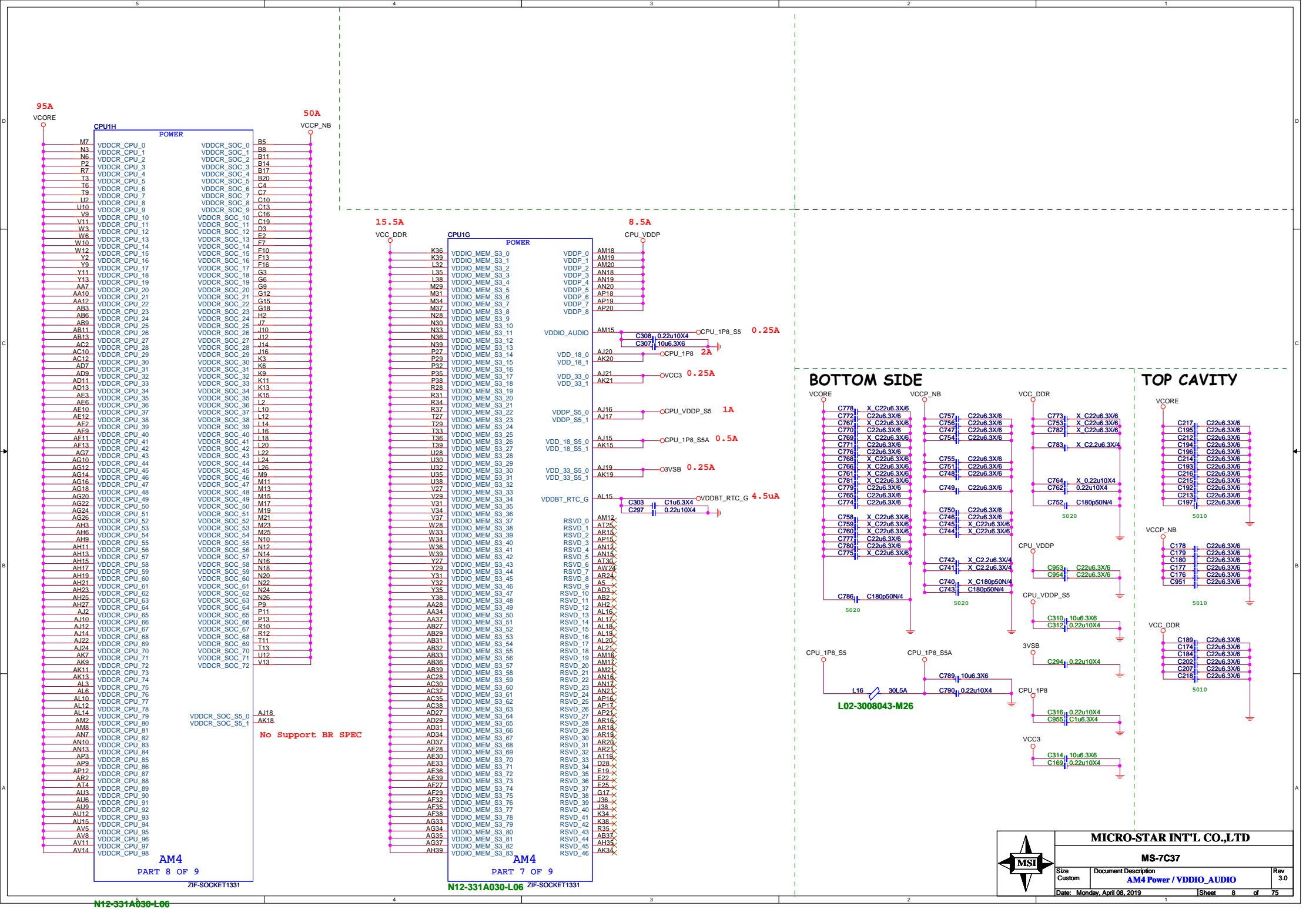
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	AM4 LPC / SPI / USB / CLK / STRAP	3.0
Date: Friday, April 12, 2019		
Sheet 7 of 75		



## SPI ROM(1.8V)







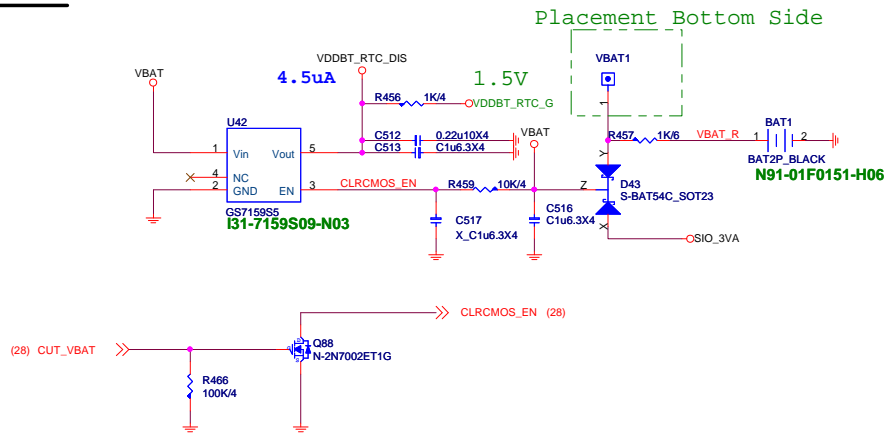


GND

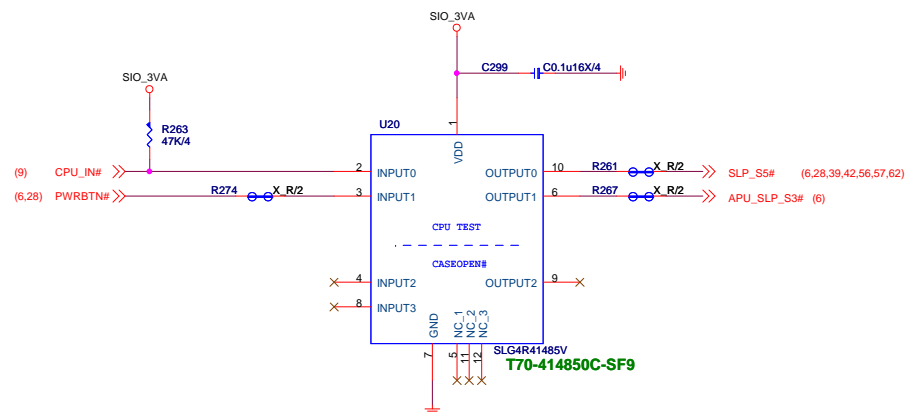
AM4  
PART 9 OF 9



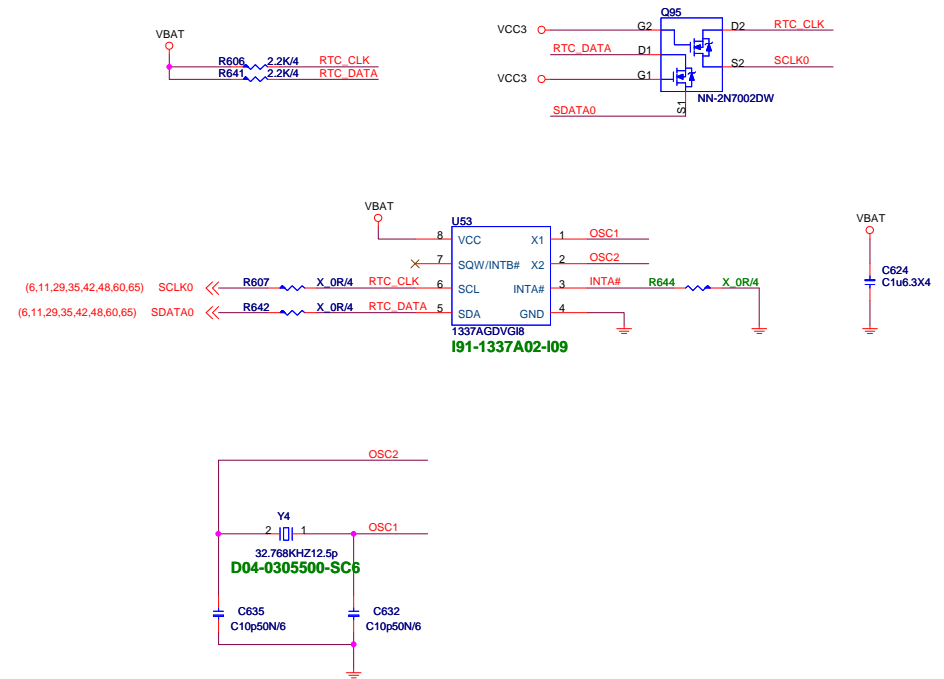
## RTC & Clear CMOS Circuit



## Clear CMOS button



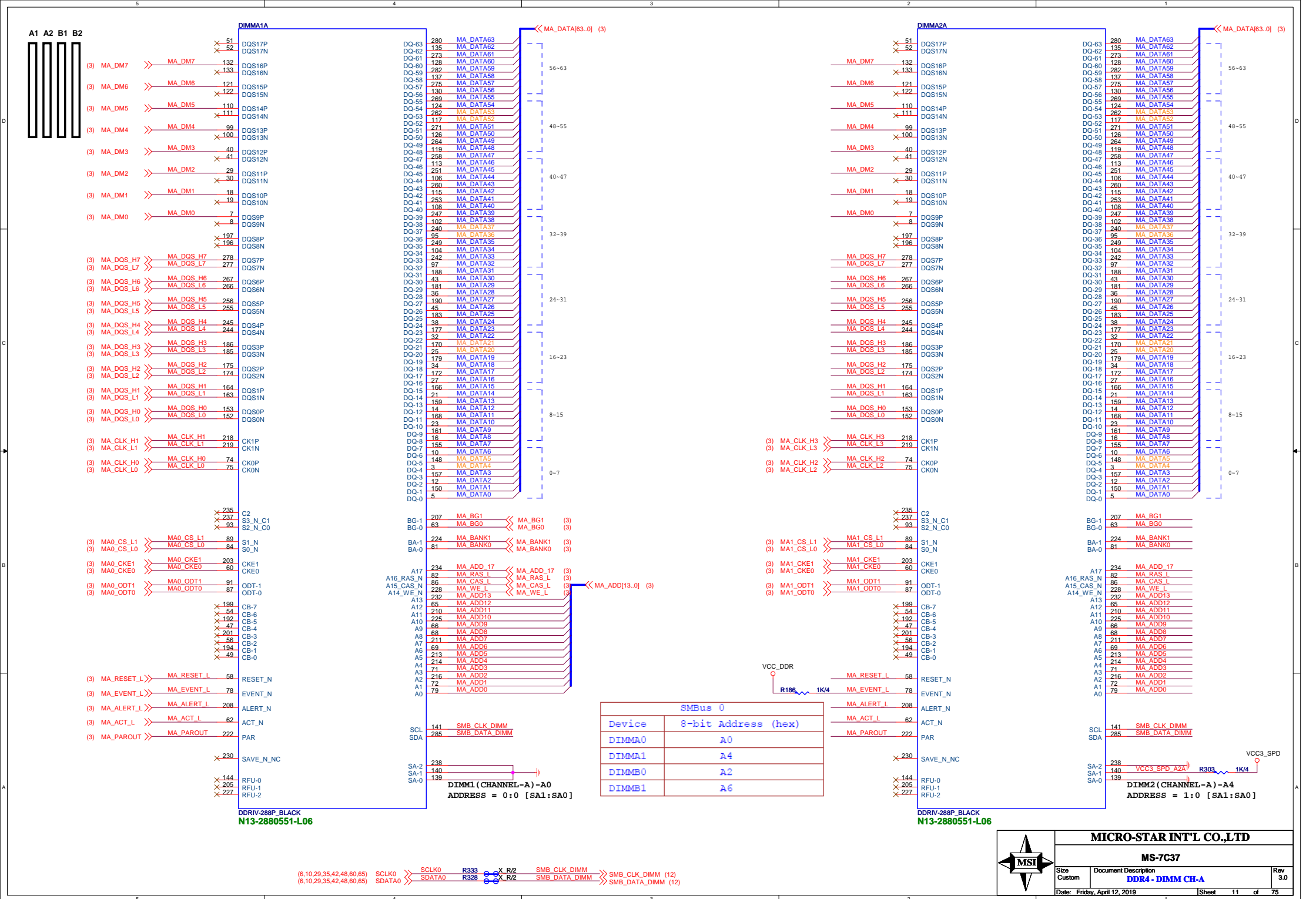
## RTC Backup

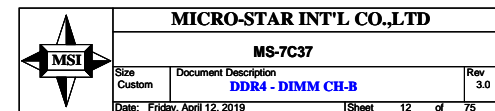


**MICRO-STAR INT'L CO.,LTD**

MS-7C37

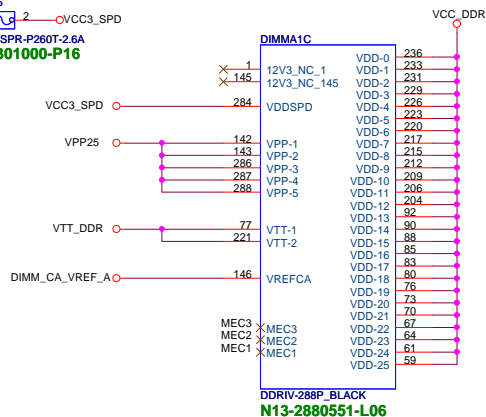
Size Custom	Document Description <b>RTC / CMOS</b>	Rev 3.0
Date: Friday, April 12, 2019 4:00 PM		Sheet 10 of 75



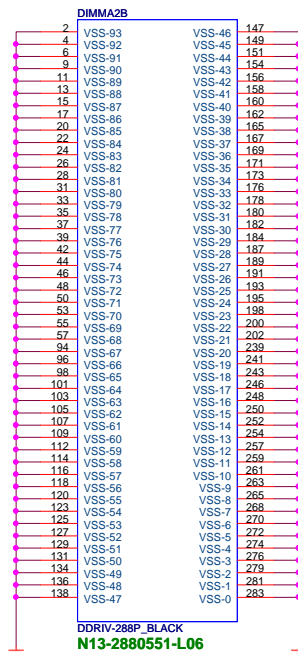
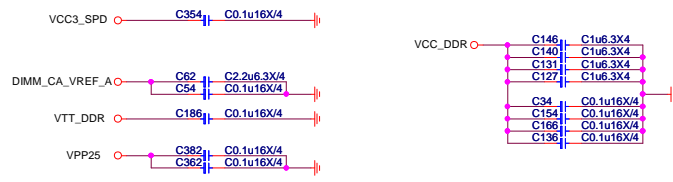
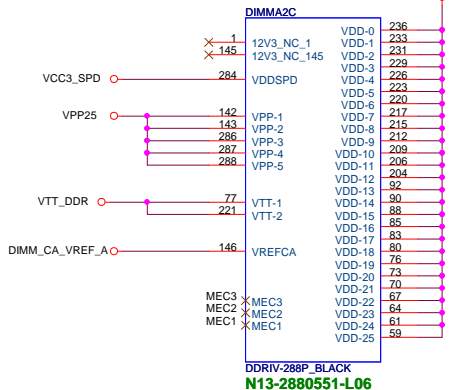
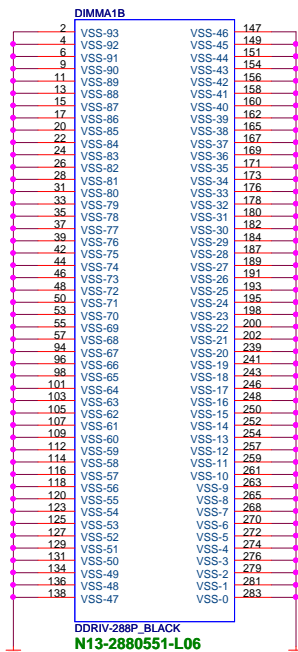
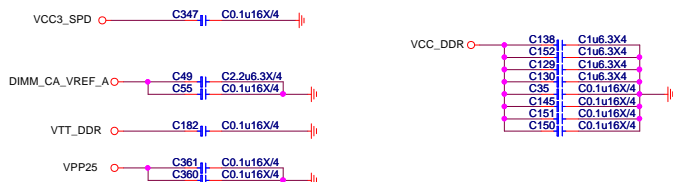


av1:D08-0301100-B07

VCC3 SPD  
F5  
F-SPR-P260T-2.6A  
D08-0301000-P16

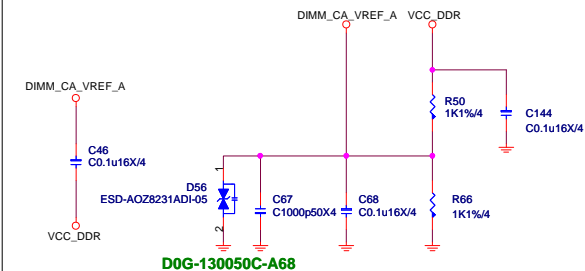


DIMM SLOT PN BY SPEC



## DDR VREF

(place resistors close to DIMMs)



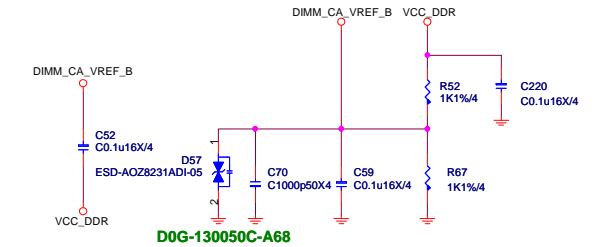
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	3.0
Date:	Monday, April 08, 2019	Sheet 13 of 75

# DDR VREF

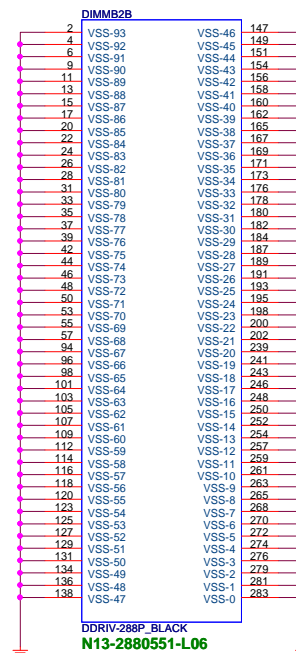
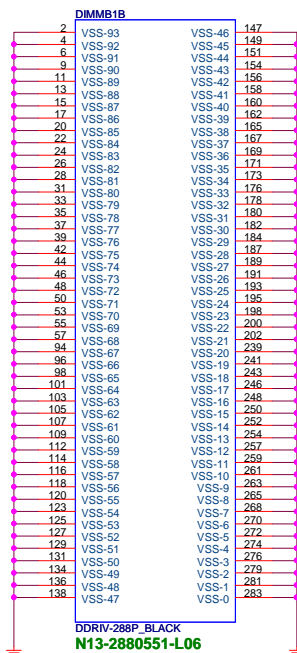
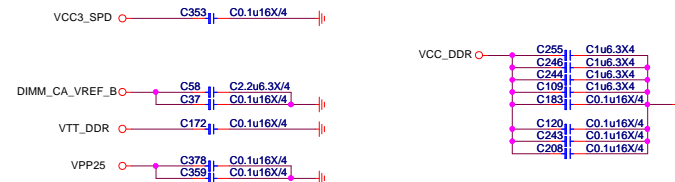
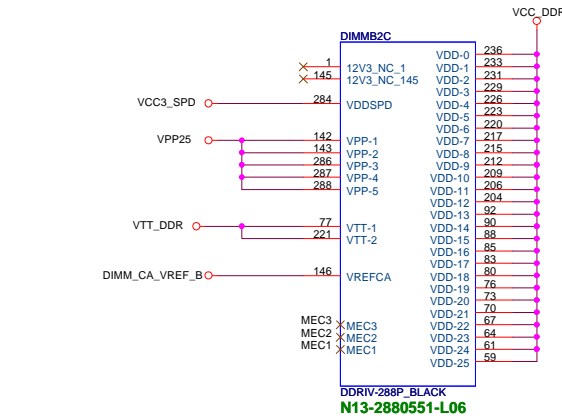
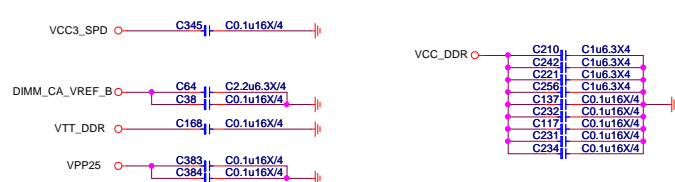
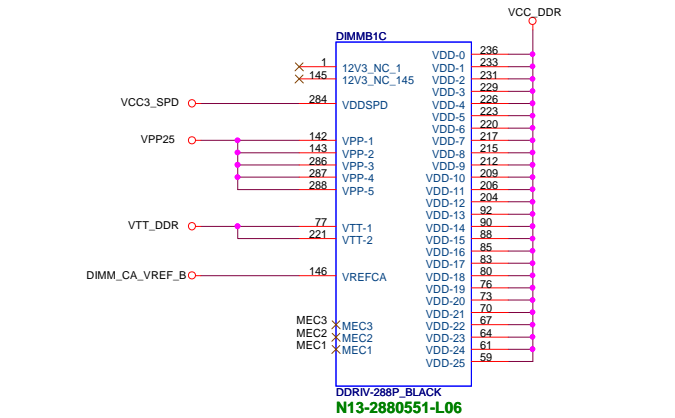
(place resistors close to DIMMs)



MICRO-STAR INT'L CO.,LTD

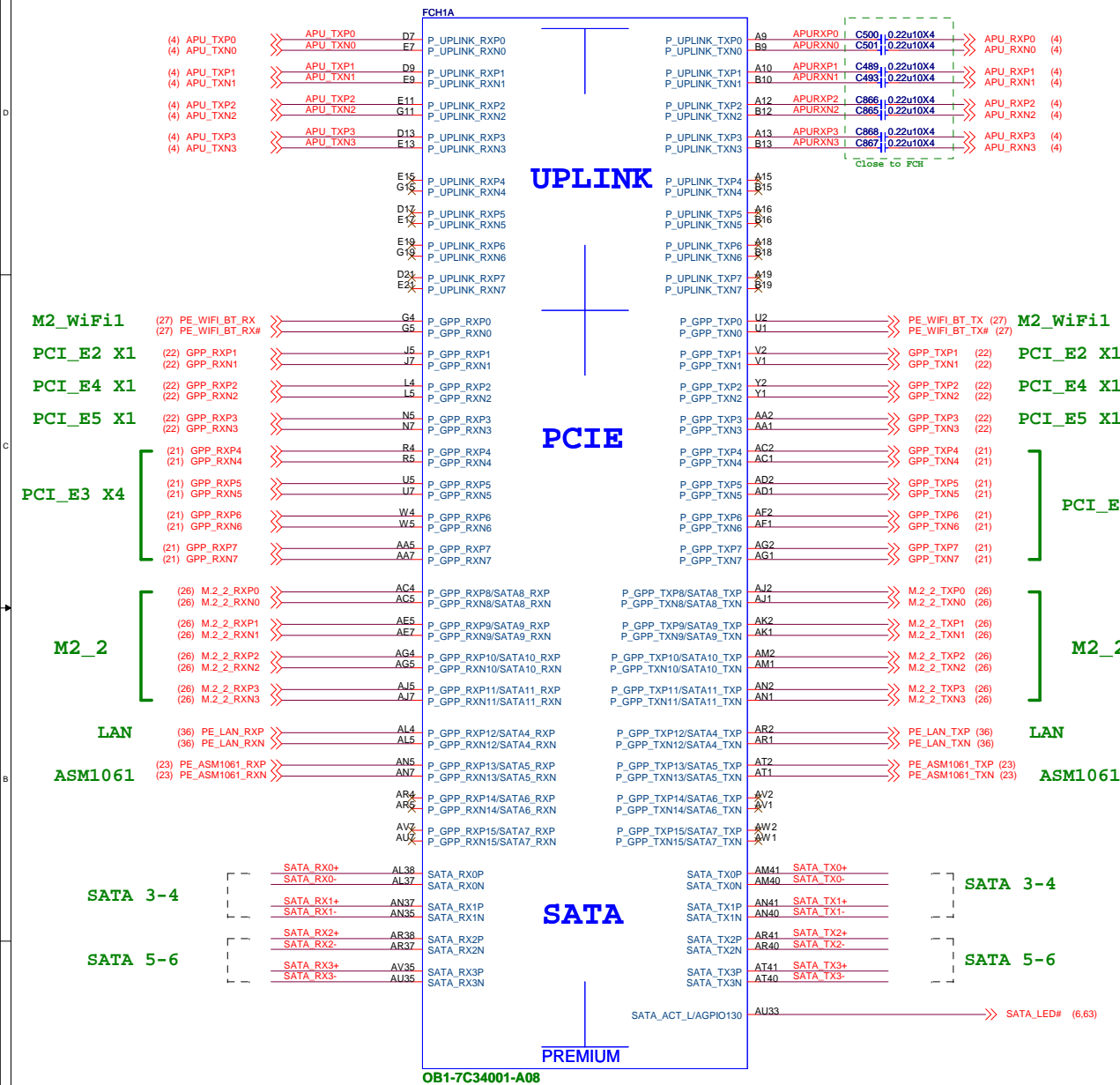
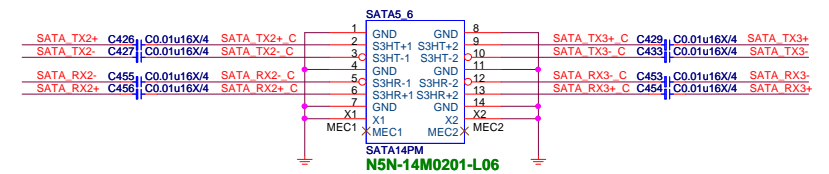
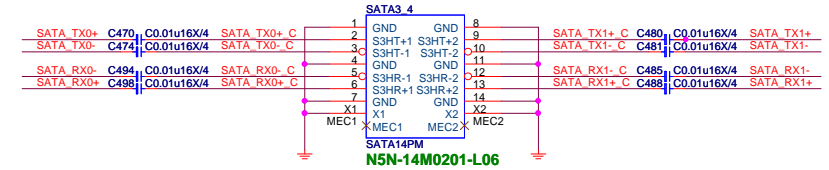
MS-7C37

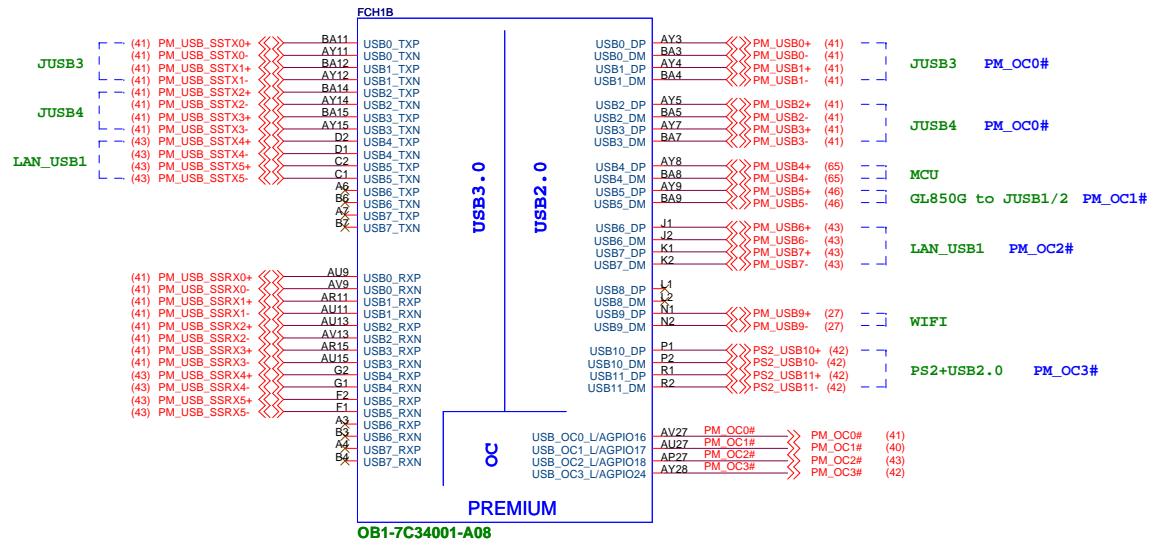
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	3.0
Date: Monday, April 08, 2019		Sheet 14 of 75



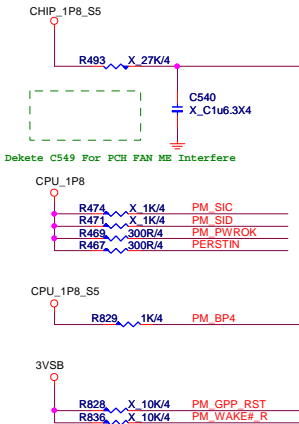
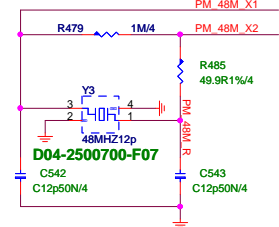
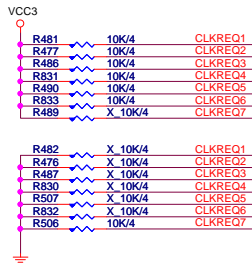


## SATA Connector

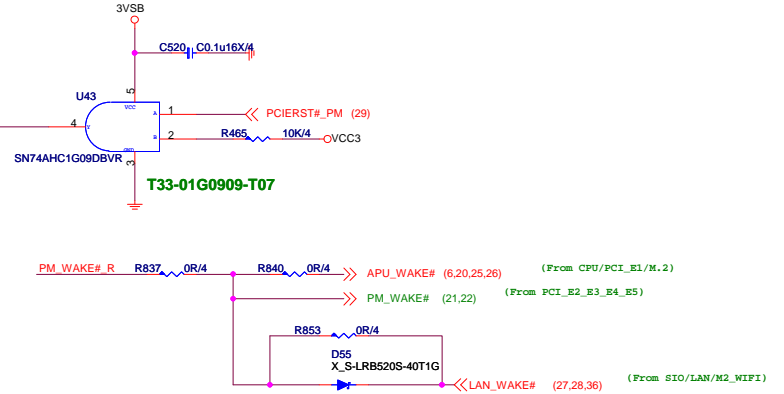
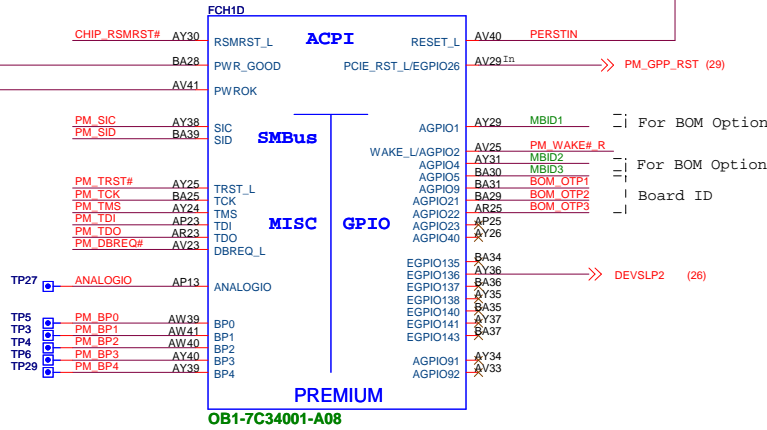
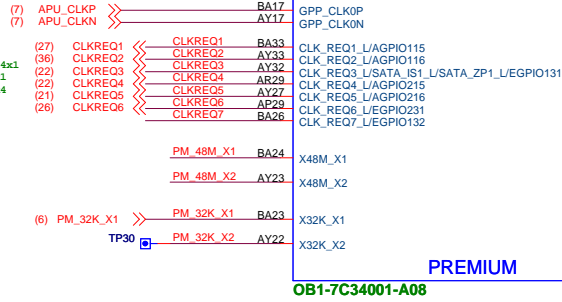




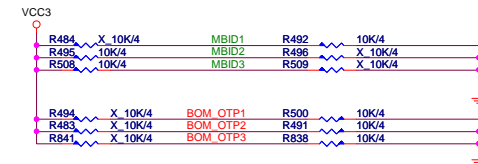
Ports	Host Controller	OC Pins Mapped
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0_L/AGPIO16 USB_OC1_L/AGPIO17
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC2_L/AGPIO18 USB_OC3_L/AGPIO24



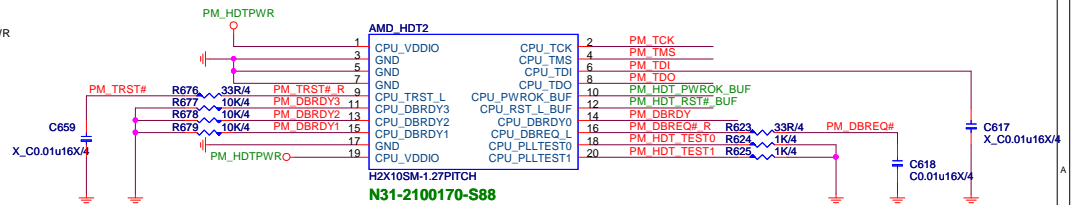
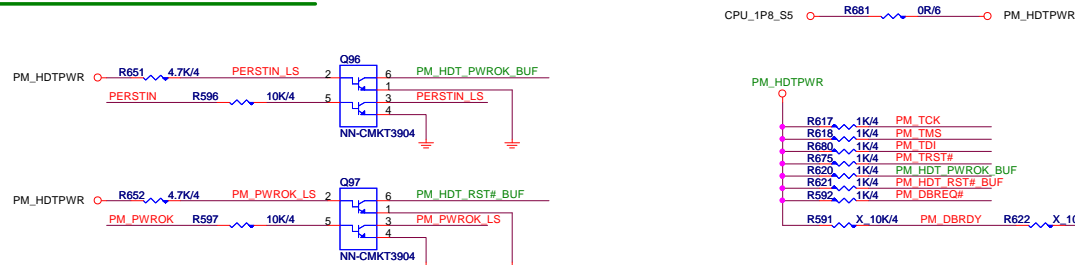
WIFI+BT  
LAN  
PCIE\_E2/4x1  
PCIE\_E5x1  
M.2.2  
ASM1061



## BOM OPTION



## PREMIUM CHIPSET\_HDT

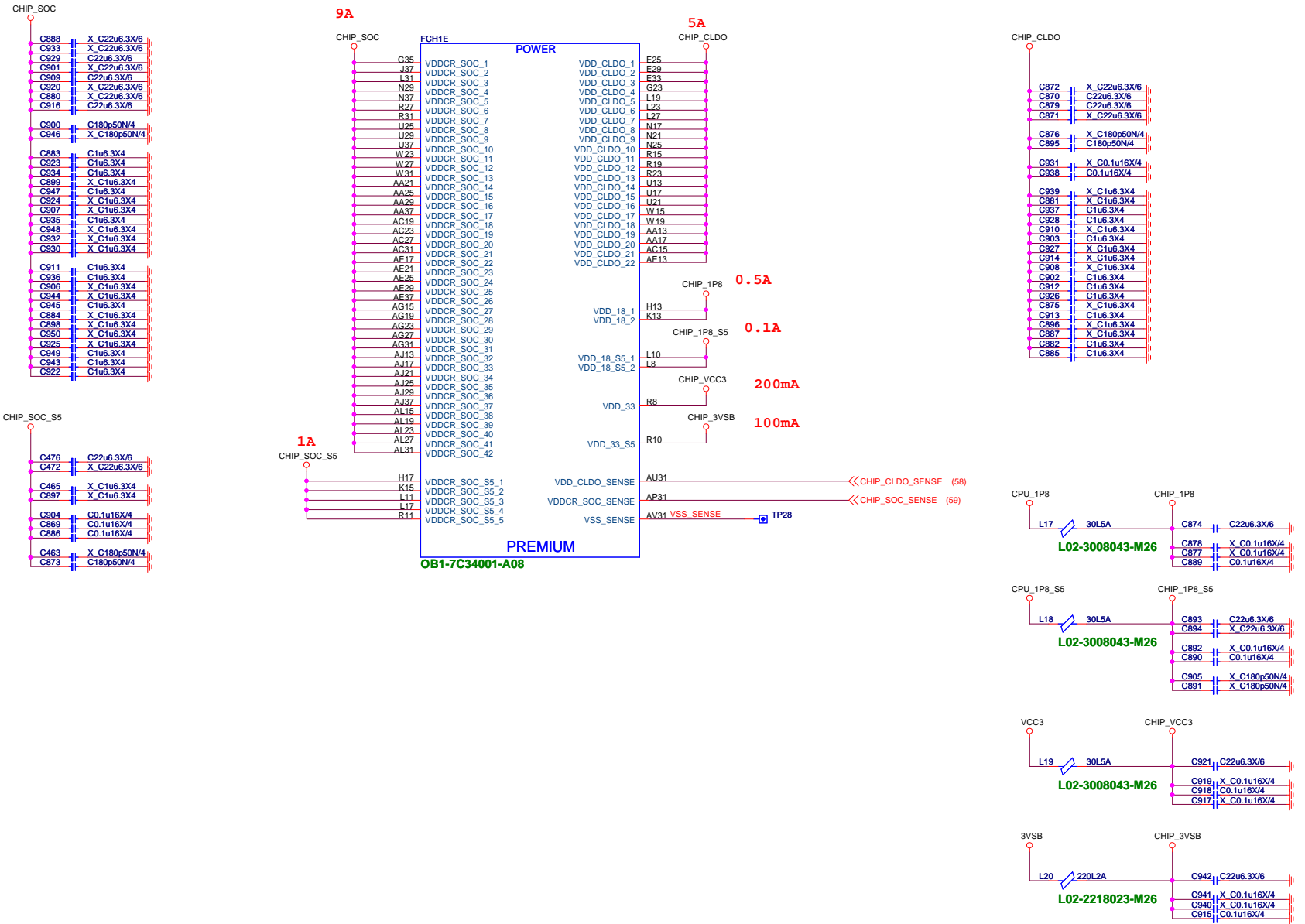


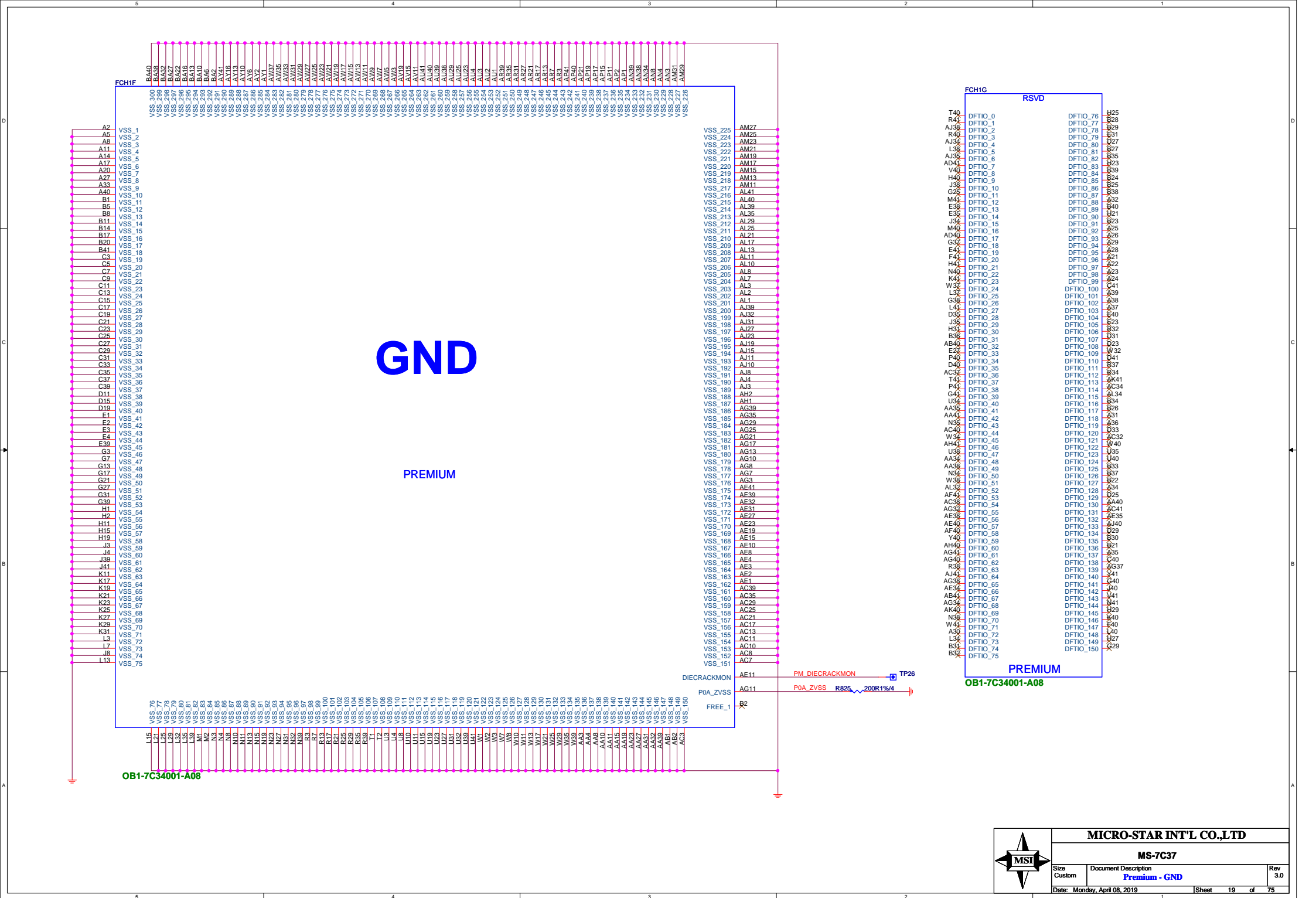
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	Premium - CLK/ACPI/GPIO	3.0
Date: Friday, April 12, 2019		Sheet 17 of 75

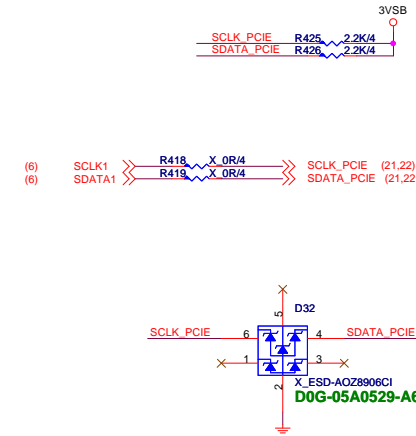
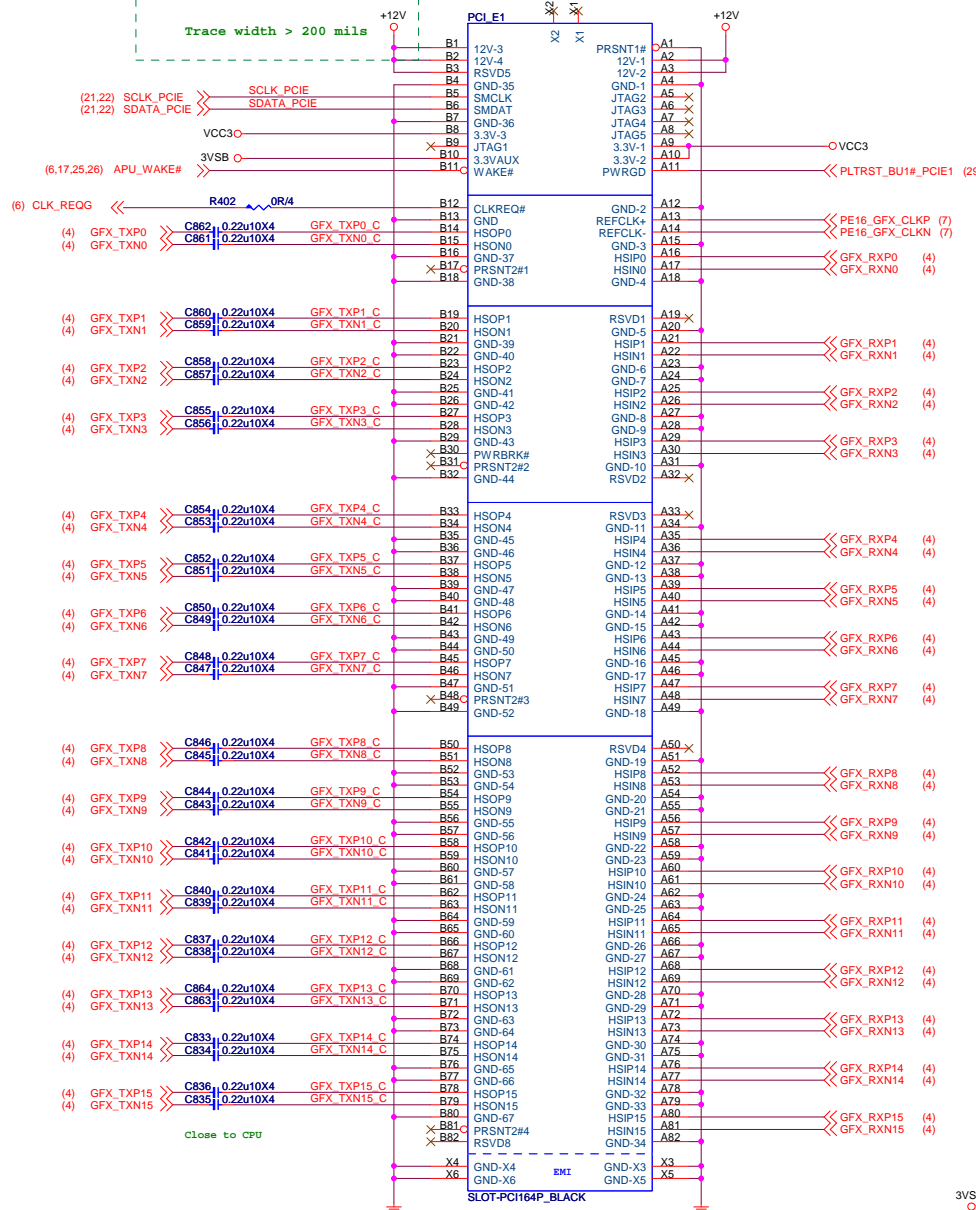
Close to FCH Power Pin





# PCI EXPRESS x16 Slot

## PCI E1



## PCI Express x16 Slot

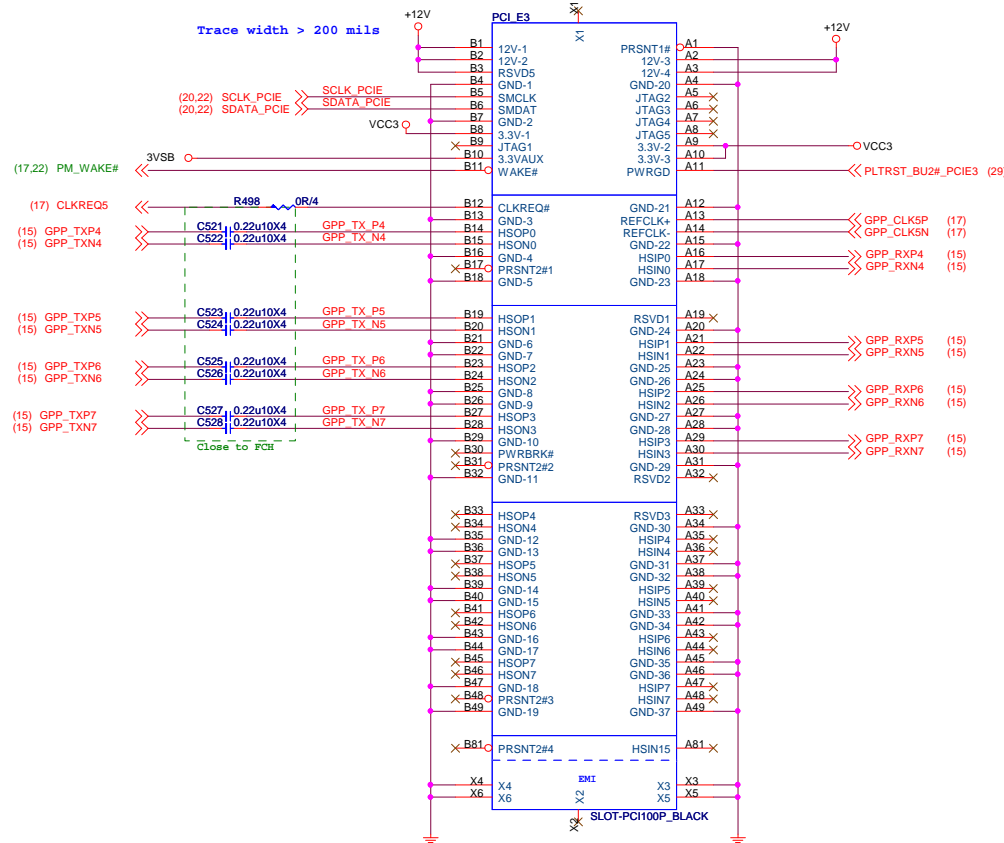
+12V	- 5.5A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 3.0
PCI_E1 (X16)		
Date: Friday, April 12, 2019	Sheet 20	of 75

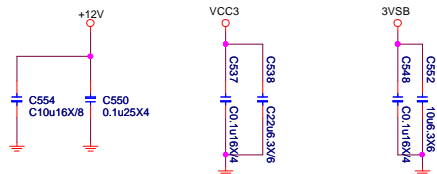


# PCI\_E3 X4



## PCI Express x4 Slot \*1

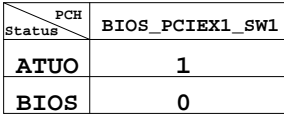
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



MICRO-STAR INT'L CO.,LTD

MS-7C37

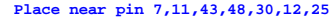
Size	Document Description	Rev
Custom	PCI_E3 (X4)	3.0
Date: Friday, April 12, 2019	Sheet 21 of 75	



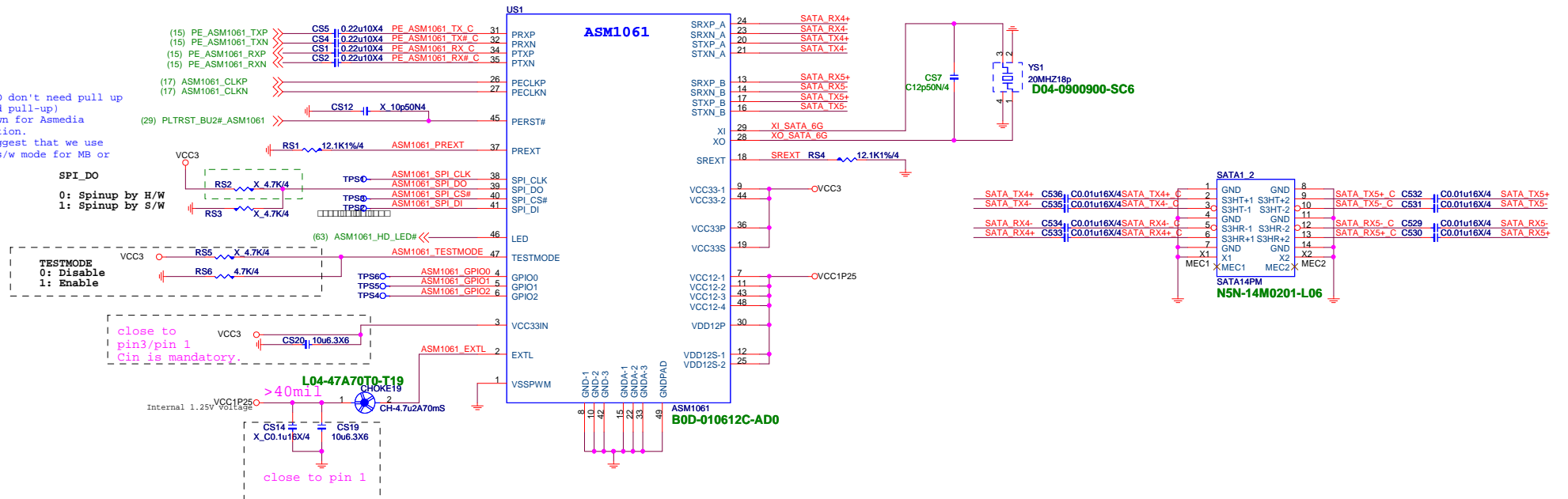
Size Custom	Document Description <b>PCIE Switch PCI_E2 / E4 / E5 (X1)</b>	Rev 3.0
Date: Friday, April 12, 2019	Sheet 22 of 75	

1.2V delay from 3.3V 90% > 0ms

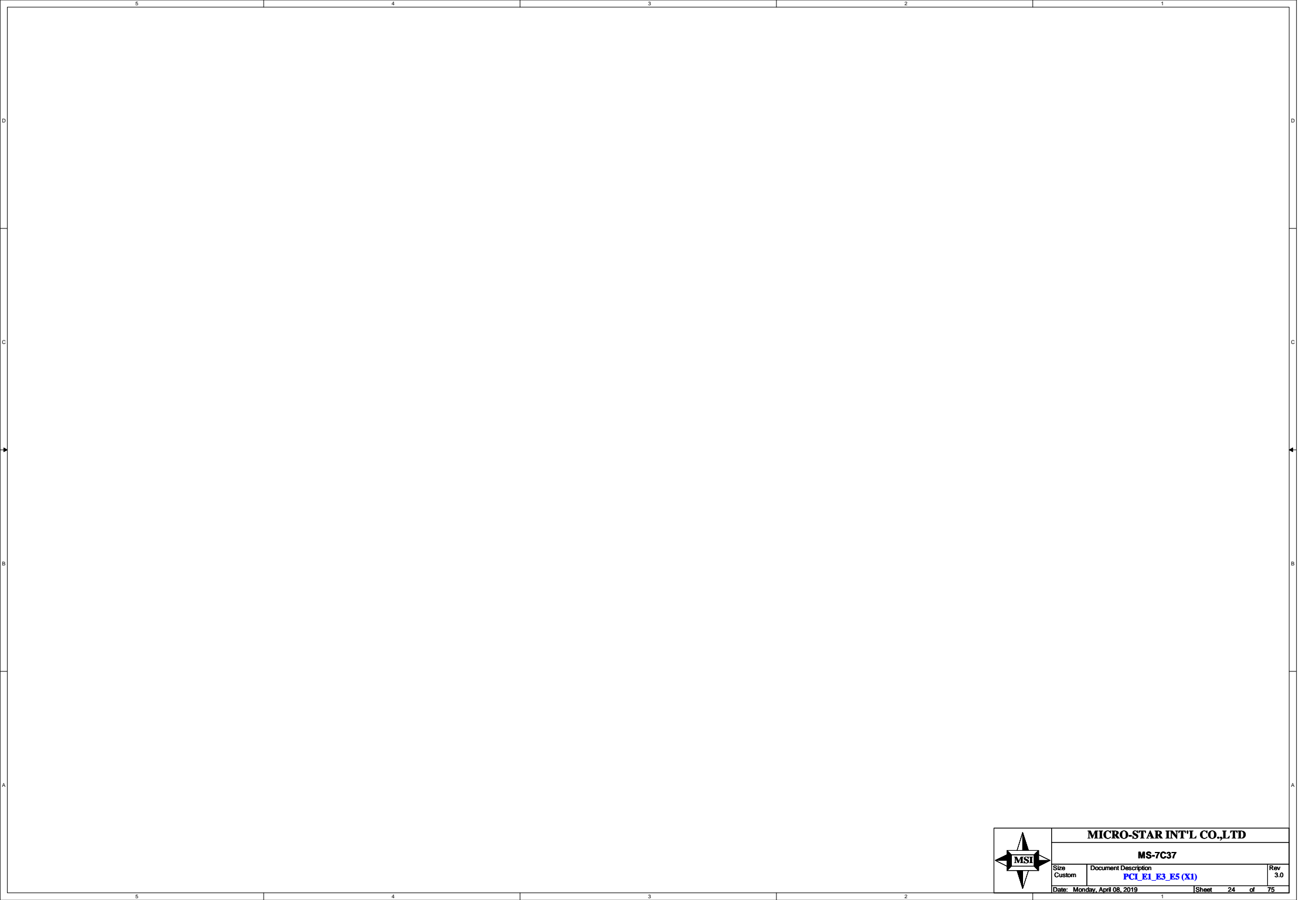
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



SATA\_SPI\_DO don't need pull up  
(integrated pull-up)  
or pull down for Asmedia  
recommendation.  
Asmedia suggest that we use  
spinup by s/w mode for MB or  
PCI-E Card.



Size Custom	Document Description <b>PCIE to SATA (ASM1061)</b>	Rev 3.0
Date: Friday, April 12, 2019		Sheet 23 of 75



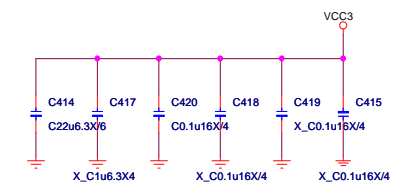
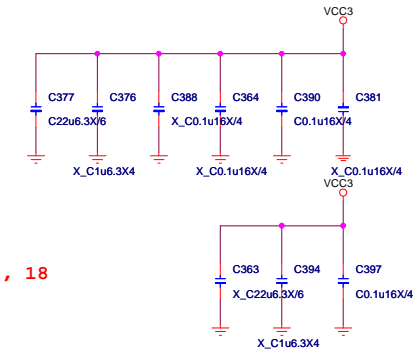
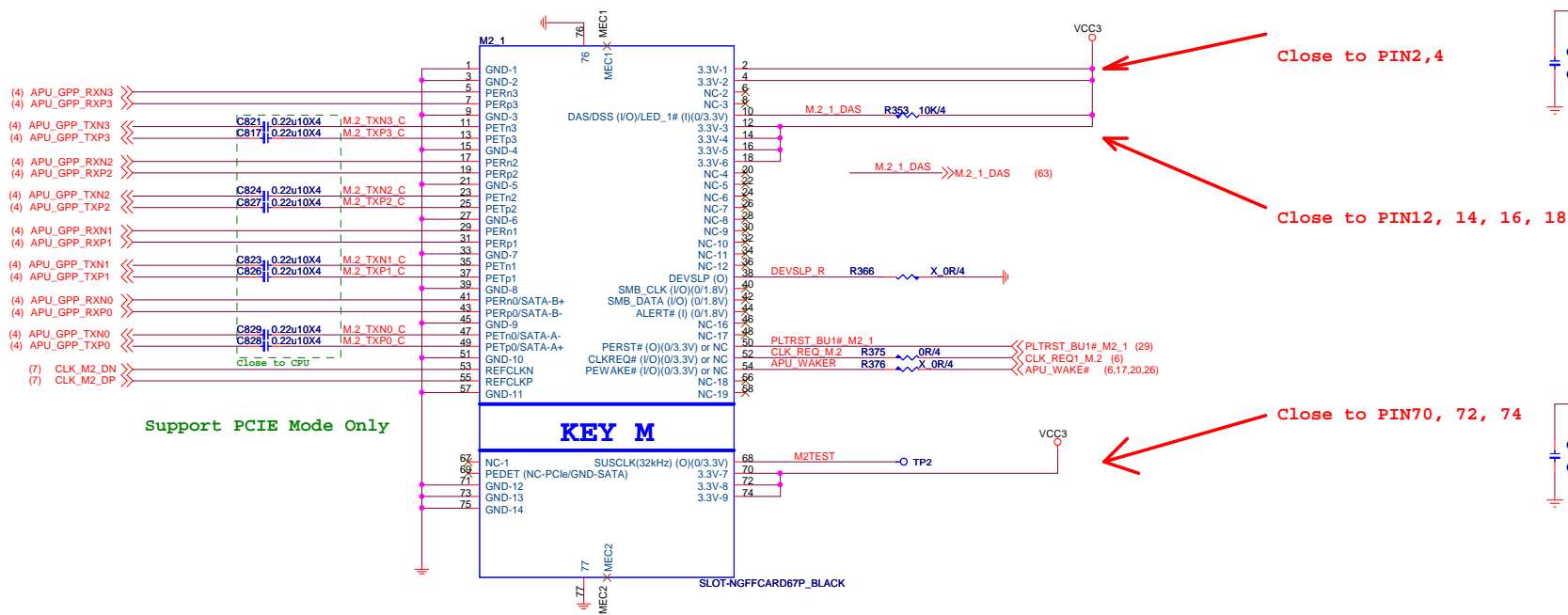
**MICRO-STAR INT'L CO.,LTD**

**MS-7C37**

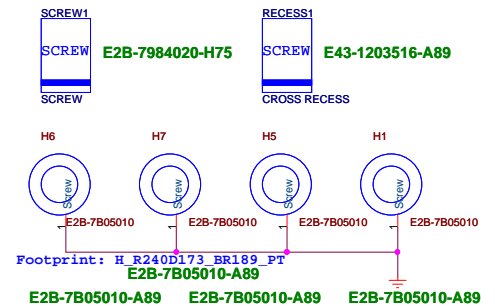
Size Custom	Document Description <b>PCI_E1_E3_E5 (X1)</b>	Rev 3.0
Date: Monday, April 08, 2019		Sheet 24 of 75

## M.2 1 Connector

VCC3 4.25A  
Max: 14W

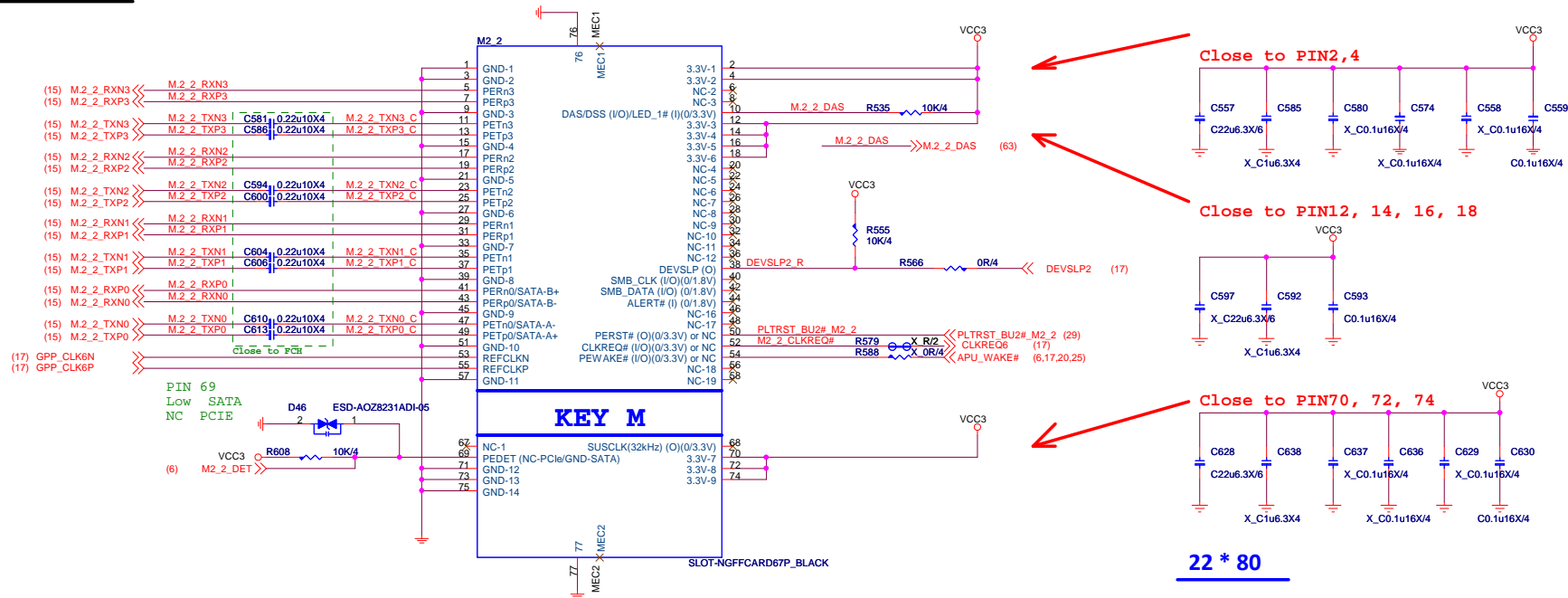


22 \* 110



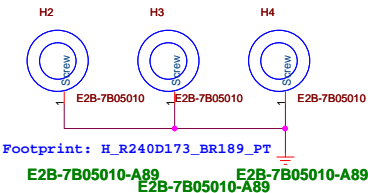
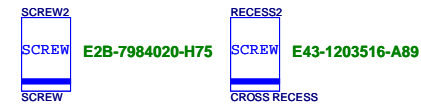
## M.2\_2 Connector

VCC3 4.25A  
Max: 14W



Support PCIE and SATA Mode

**22 \* 80**



**MICRO-STAR INT'L CO.,LTD**

MS-7C37

Size Custom	Document Description <b>M2_2</b>	Rev 3.0
Date: Friday, April 12, 2019		Sheet 26 of 75







SIO HM Voltage over 2.048V will not detect

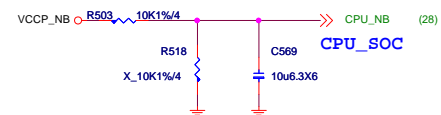
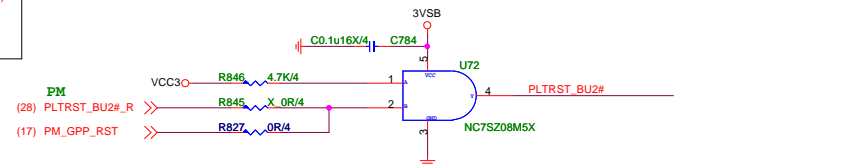


Diagram illustrating the CPU MOS bypass network. The circuit includes resistors R513 (10K1%/4) and RT4 (10K1%/4), and capacitors C553 (C2200p/50%/4) and C2200p. The network is connected to HM\_VREF, CPUMOSTIN, and GNDHIM. A note indicates that C553 should be placed close to the CPU MOS.

[illegible]

SIO (28) PLTRST\_BU2#\_R >> R595 X 22R1%/4 PLTRST\_BU2# R387 100R1%/4 PLTRST\_BU2#\_LAN (36) R571 100R1%/4 PLTRST\_BU2#\_ASM1061 (23)



PCIE\_RST# R478 X R/2 PCIE\_RST\_BUF

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$



MS-7C37

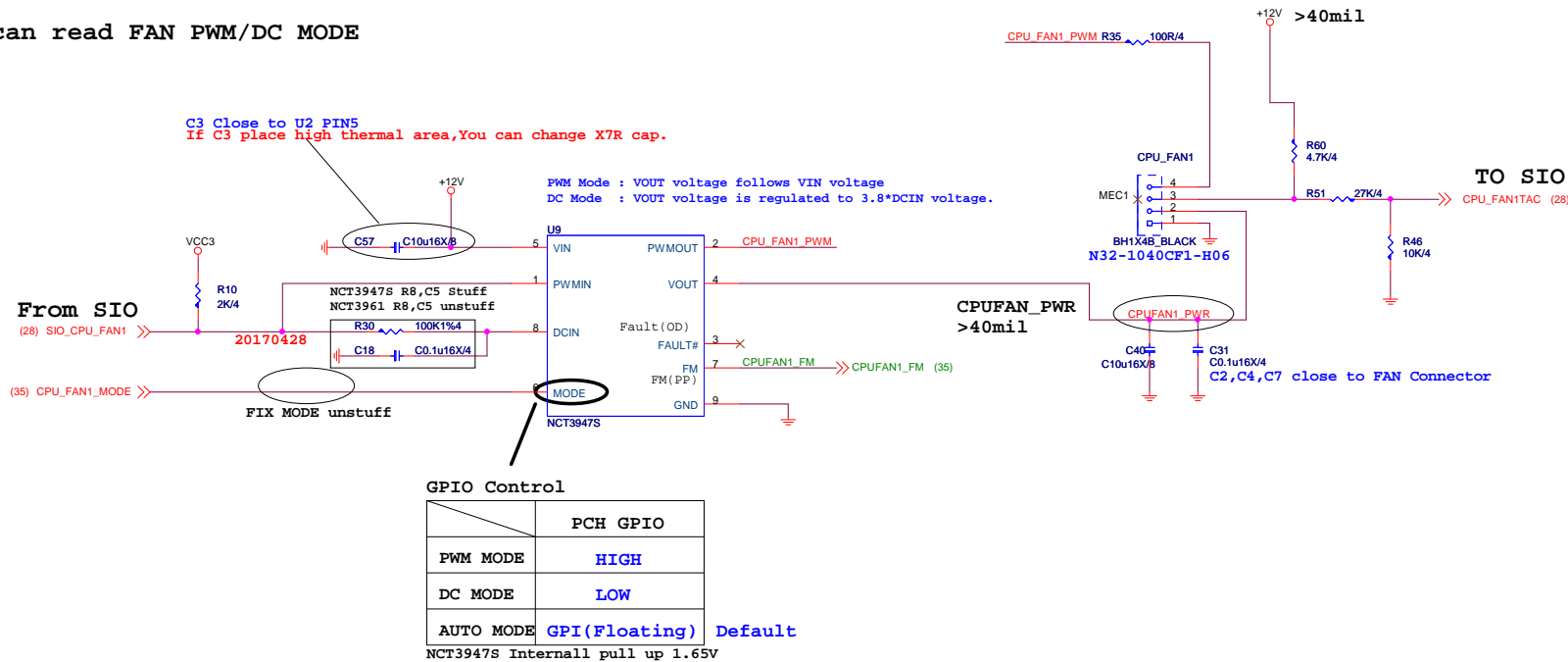
Size Custom	Document Description <b>SIO - HW Monitor / NCT7718W</b>	Rev 3.0
Date: Friday, April 12, 2019	Sheet 29 of 75	

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

## CPUFAN1

- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



## PUMPFAN1

[illegible]

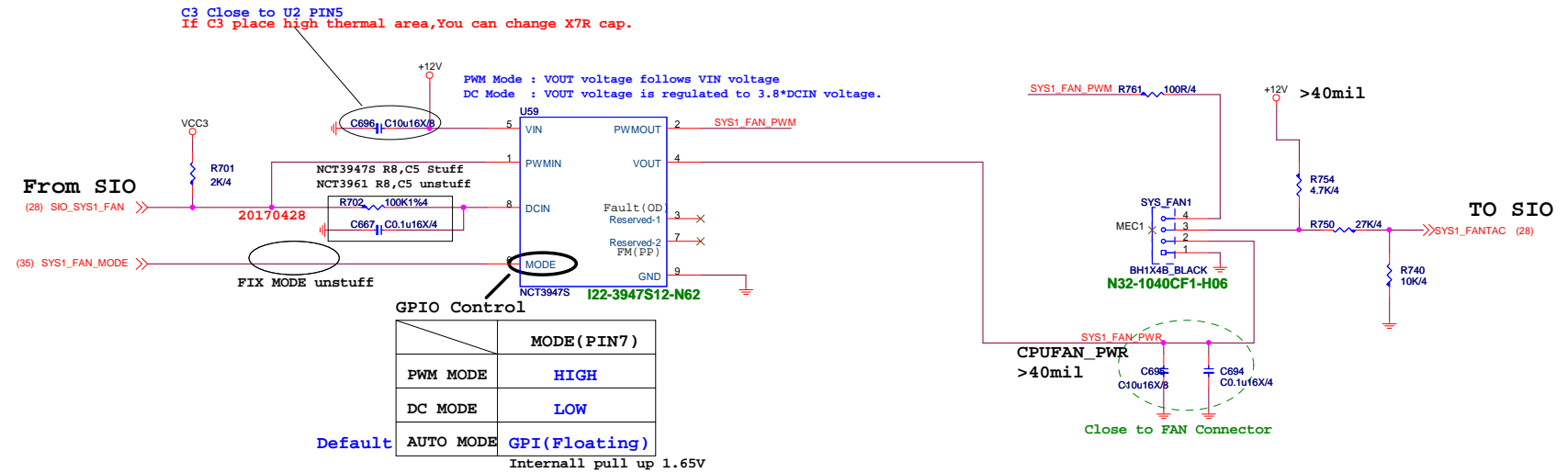
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

NCT3947S Internall pull up 1.65V

## SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

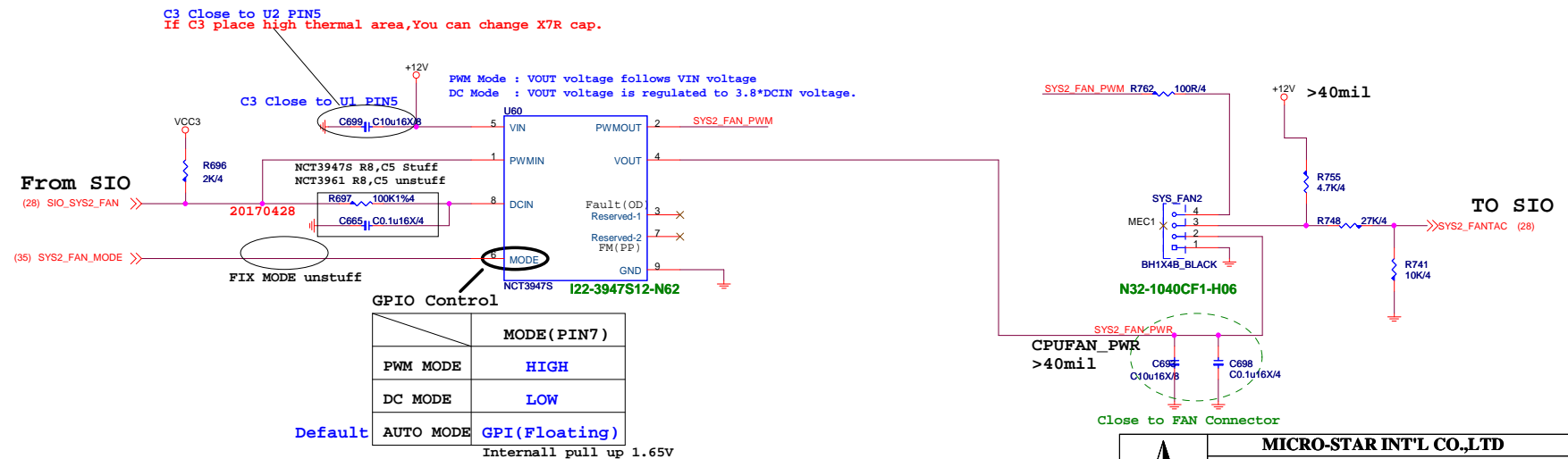
1.Mode GPIO BIOS can swtich PWM/DC MODE



## SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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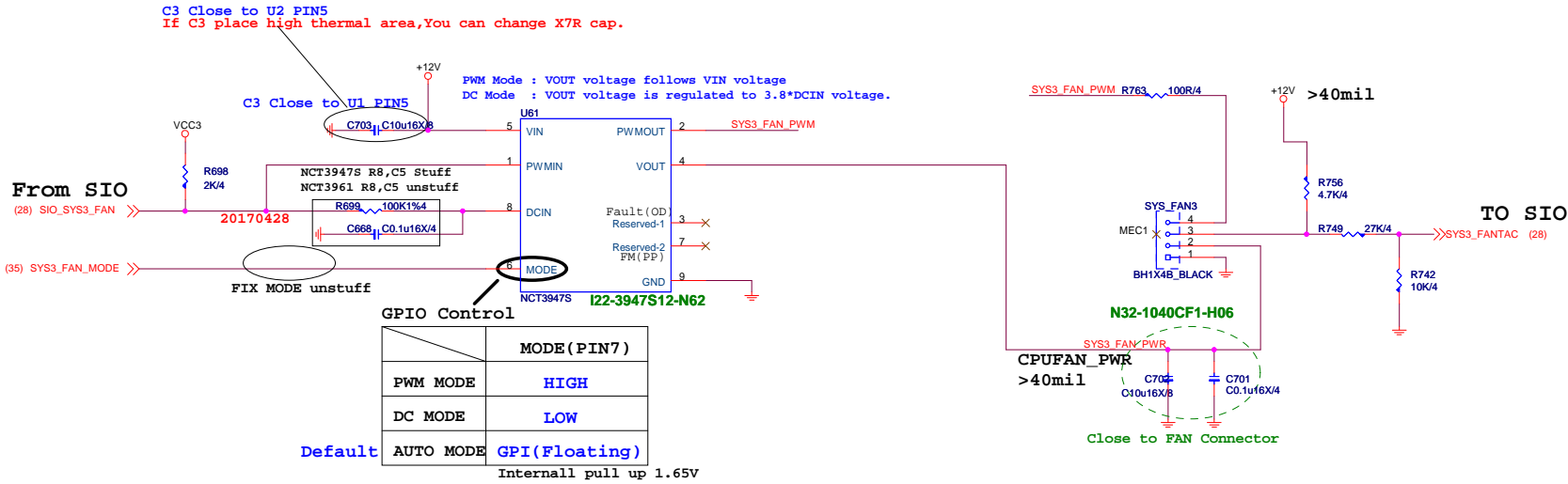
Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	3.0
Date: Friday, April 12, 2019		Sheet 32 of 75



SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

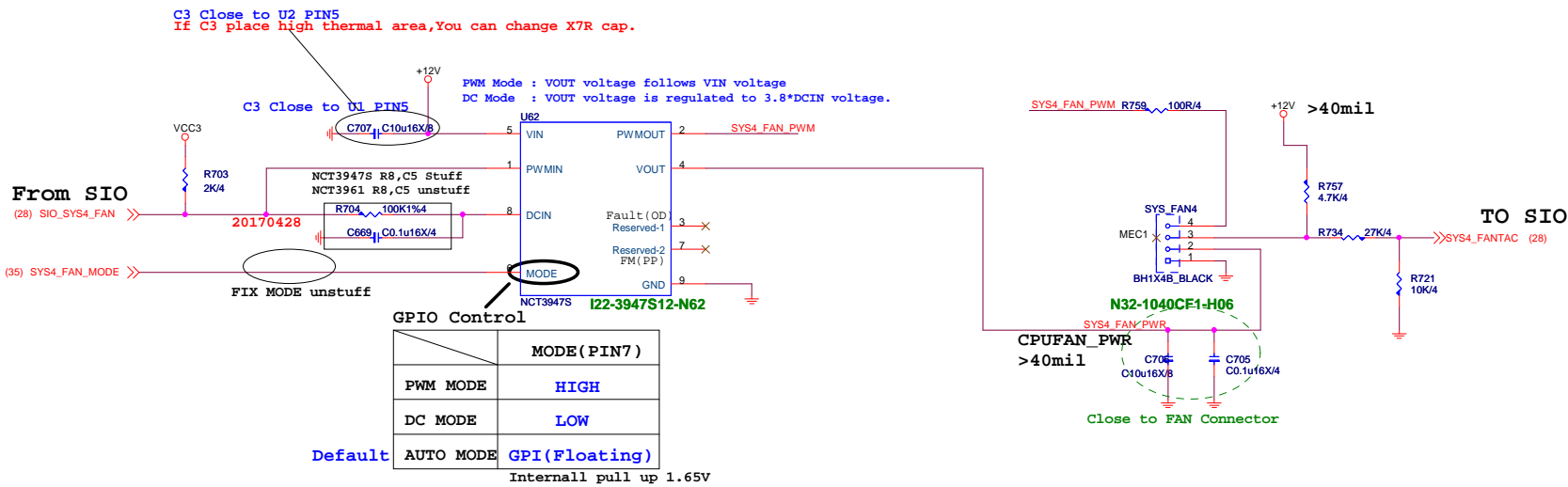
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

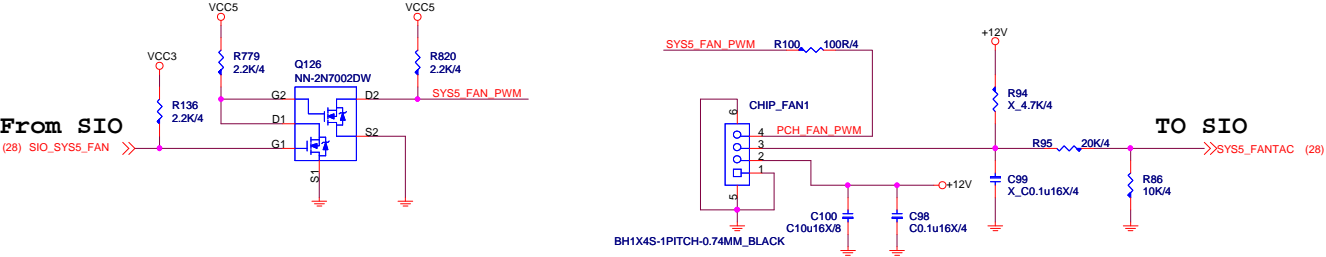


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Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	3.0
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PCH\_FAN



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Size Custom	Document Description <b>PCH_FAN</b>	Rev 3.0
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By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE  
Default GPI

BIOS SHOW FAN MODE Information USE  
Default GPI

use avoid S5 leakage

CPUFAN1\_FM R47 1K/4

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

By PM Define FAN name

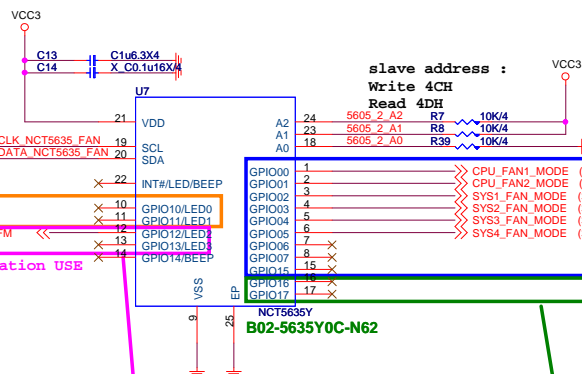
LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2



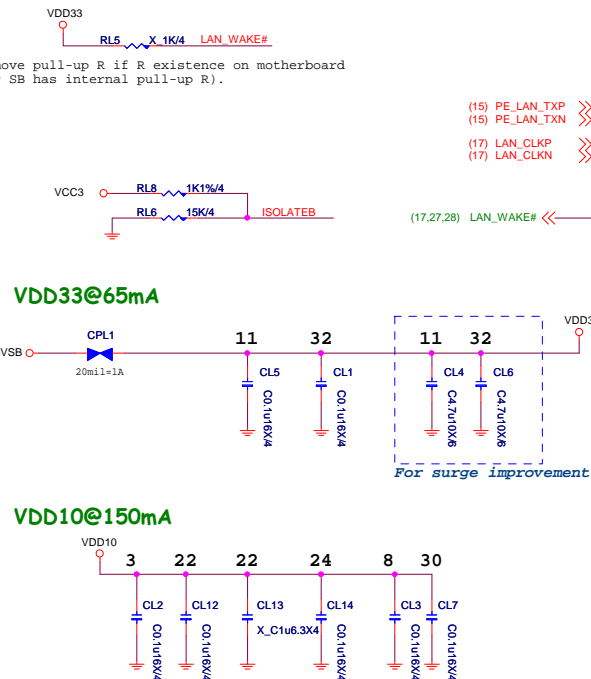
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size Custom	Document Description FAN GPIO NCT5635	Rev 3.0
Date: Friday, April 12, 2019	Sheet 35 of 75	

# RTL8111H Giga LAN

Remove pull-up R if R existence on motherboard  
(or SB has internal pull-up R).



Pull-up resistor RL9 required to either  
3.3V suspend or core rail depending on  
the power well of the PCH input CLKREQ# buffer.

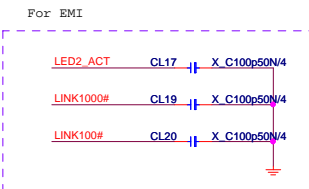
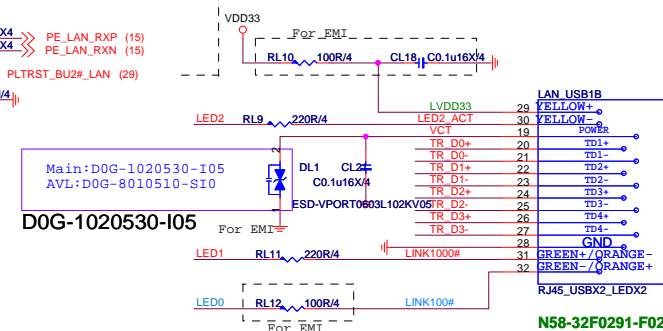


8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

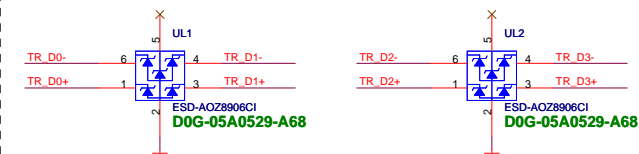
PIN19:  
AMD platform connect to PCIE\_RST#,  
don't connect to A-RST#.  
INTEL platform connect to PLT\_RST#,

## LAN Connector



## ESD Protect close to connector

D0G-0200529-A68  
D0G-0100619-I05



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Size	Document Description	Rev
Custom	LAN - I211AT	3.0
Date: Friday, April 12, 2019	Sheet 36 of 75	

The diagram illustrates the pin connections for the C91-1011031-P01 microcontroller, categorized into Digital and Analog sections.

**Digital Section:**

- Pin 7:** BCLK
- Pin 8:** SYNC
- Pin 9:** SDATA-IN
- Pin 10:** SDATA-OUT
- Pin 11:** GPIO4/EAPD/MIC-GPI
- Pin 12:** GPIO6/MIC-GPI/EAPD
- Pin 13:** SPDIF-OUT/MIC-GPI
- Pin 14:** LED-BEAT/GPIO0/DMIC-DAT12
- Pin 15:** EAPD/GPIO1/DMIC-CLK/LD-PULSE
- Pin 16:** DVDD
- Pin 17:** DVDD-IO
- Pin 18:** LDO3\_CAP
- Pin 19:** GND\_PAD

**Analog Section:**

- Pin 20:** CPVDD
- Pin 21:** CPVEE
- Pin 22:** AVDD1
- Pin 23:** LDO1\_CAP
- Pin 24:** LDO2\_CAP
- Pin 25:** LDO2\_VRP
- Pin 26:** VREF

**Power Supply Connections:**

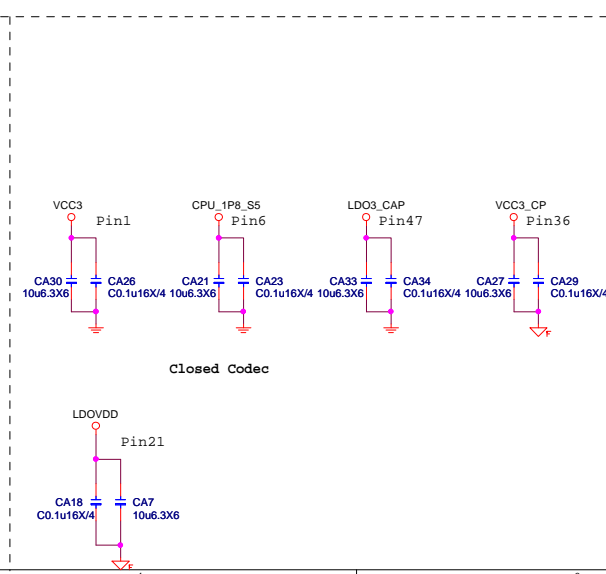
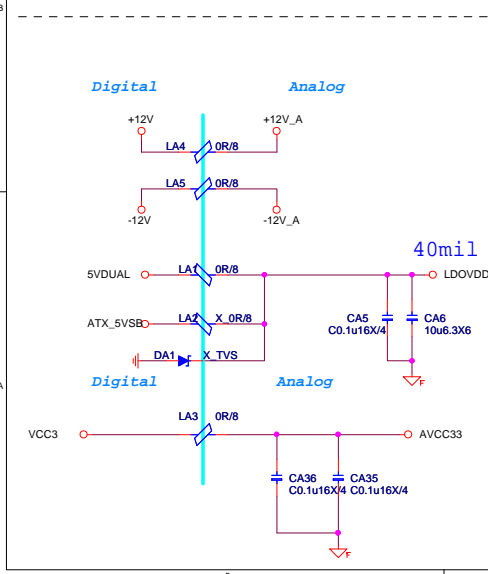
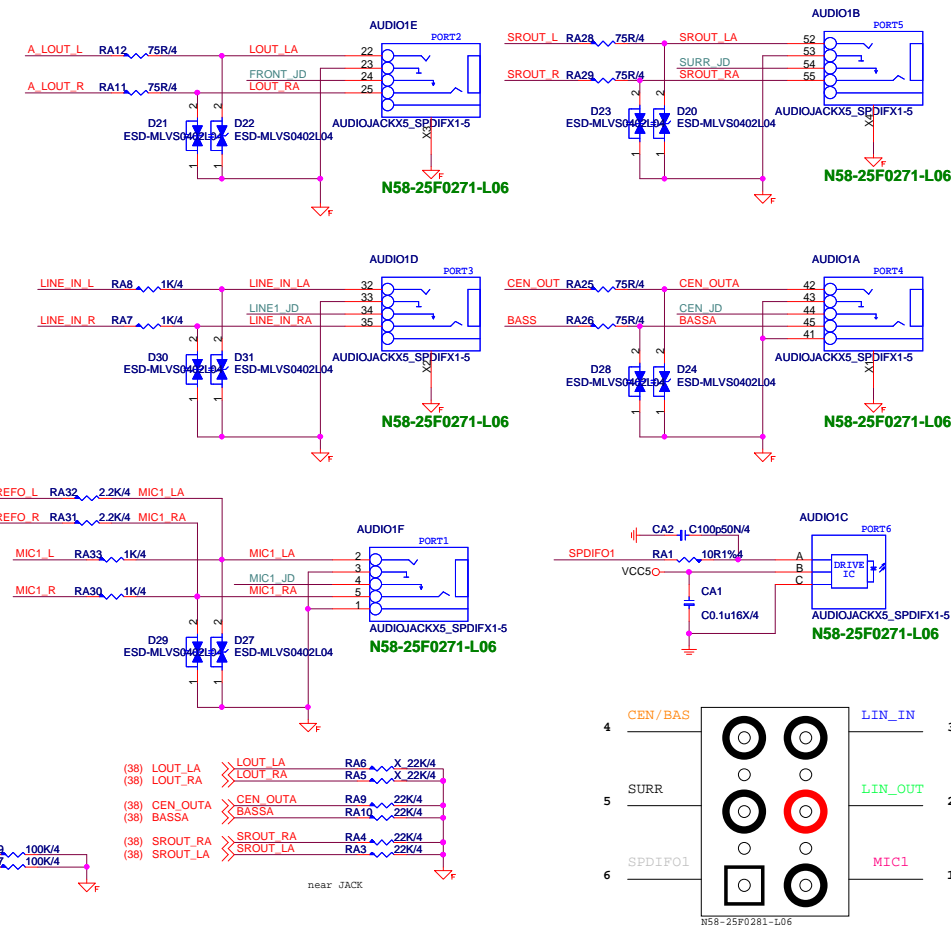
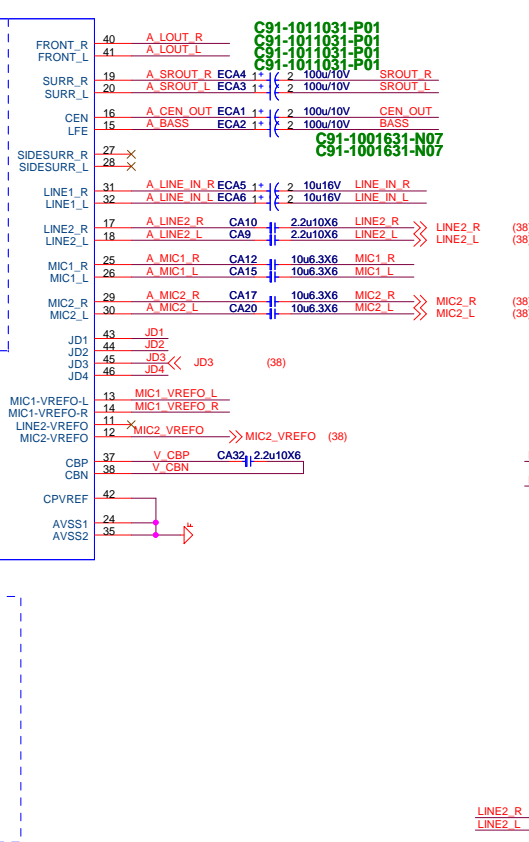
- VCC3\_0N4:** Connected to Pin 11 (GPIO4/EAPD/MIC-GPI).
- VCC3\_CP:** Connected to Pin 20 (CPVDD).
- V\_LDO1\_CAP:** Connected to Pin 23 (LDO1\_CAP).
- V\_LDO2\_CAP:** Connected to Pin 24 (LDO2\_CAP).
- V\_LDO2\_VRP:** Connected to Pin 25 (LDO2\_VRP).
- VREF:** Connected to Pin 26 (VREF).

**Package Connections (C91-1011031-P01):**

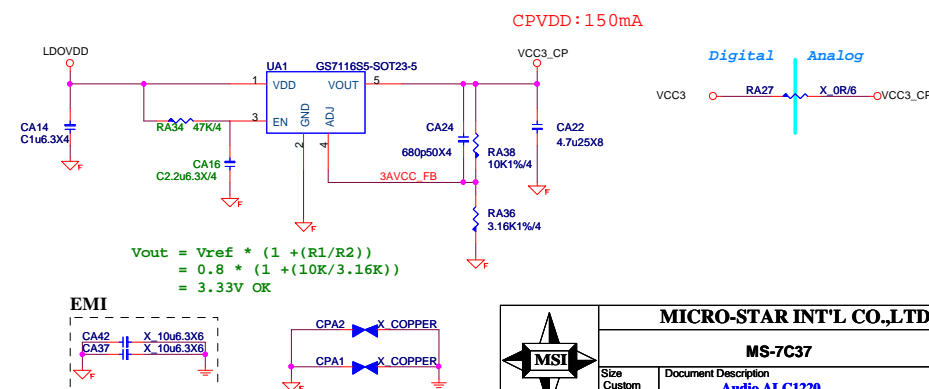
- AVCC33:** Connected to Pin 16 (DVDD).
- RA41:** Connected to Pin 17 (DVDD-IO).
- RA46:** Connected to Pin 18 (LDO3\_CAP).
- RA44:** Connected to Pin 19 (GND\_PAD).
- RA45:** Connected to Pin 20 (CPVDD).
- RA39:** Connected to Pin 21 (CPVEE).
- RA42:** Connected to Pin 22 (AVDD1).
- RA40:** Connected to Pin 23 (LDO1\_CAP).
- RA43:** Connected to Pin 24 (LDO2\_CAP).
- RA2:** Connected to Pin 25 (LDO2\_VRP).
- LINE1\_JD:** Connected to Pin 26 (VREF).

**Notes:**

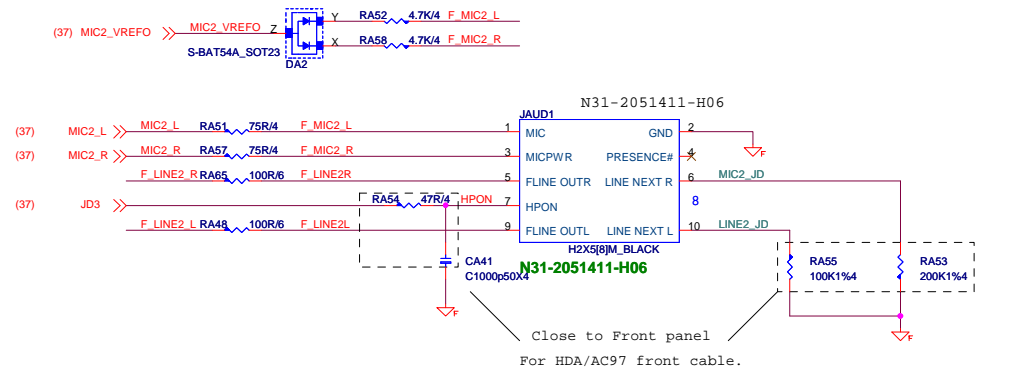
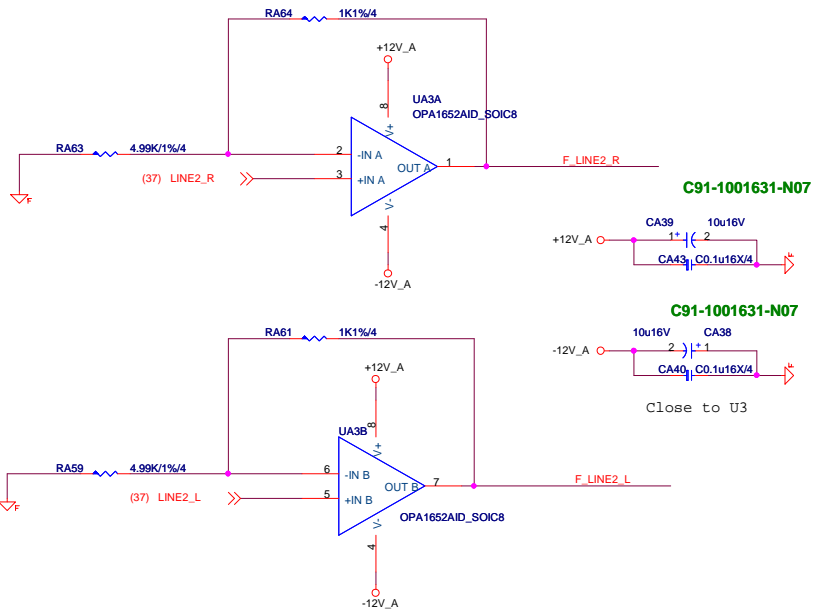
- Pin 11 is also connected to CA19 and X\_10p50N4.
- Pin 12 is also connected to SPDIF01.
- Pin 13 is also connected to EAPD.
- Pin 14 is also connected to DVDD.
- Pin 15 is also connected to DVDD-IO.
- Pin 16 is also connected to LDO3\_CAP.
- Pin 17 is also connected to GND\_PAD.
- Pin 18 is also connected to CPVDD.
- Pin 19 is also connected to CPVEE.
- Pin 20 is also connected to AVDD1.
- Pin 21 is also connected to LDO1\_CAP.
- Pin 22 is also connected to LDO2\_CAP.
- Pin 23 is also connected to LDO2\_VRP.
- Pin 24 is also connected to VREF.



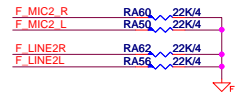
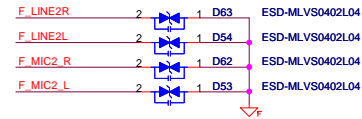
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



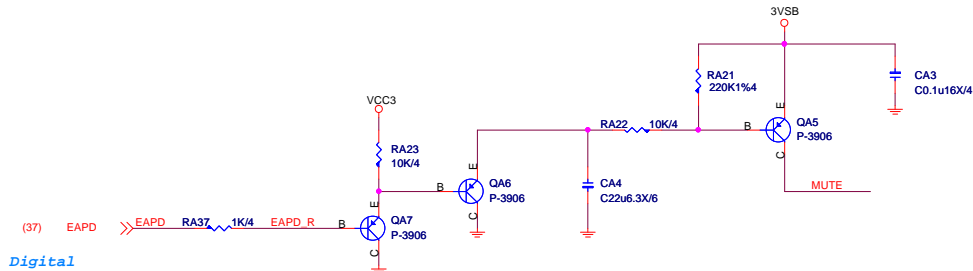
<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7C37</b>			
Size Custom	Document Description <b>Audio ALC1220</b>	Rev 3	
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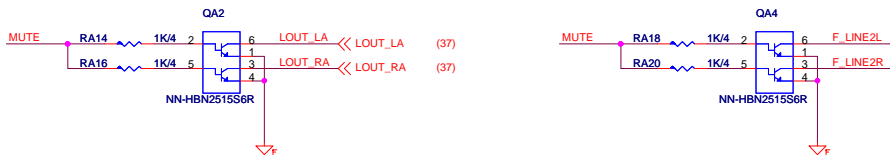
Close to Jack  
ESD protect



### Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

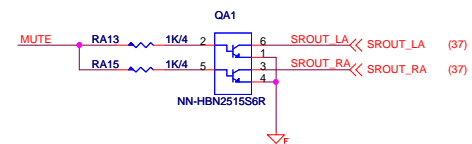
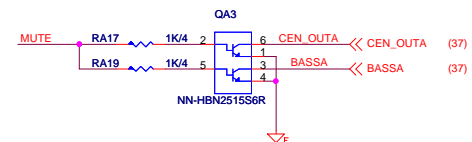


Analog

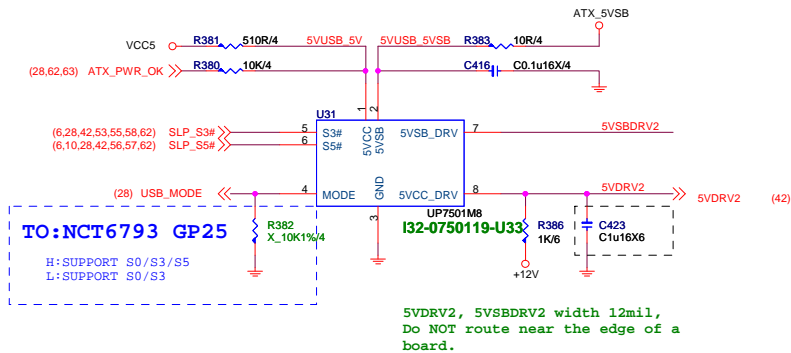


Audio moat is transparent and width 40mil

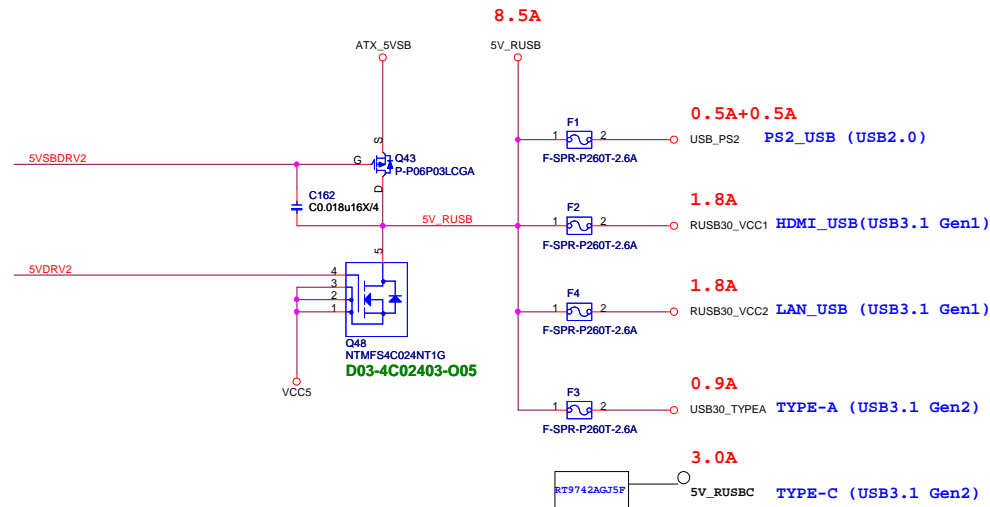
(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change SROUT\_LA, SROUT\_RA, CEN\_OUTA, BASSA to TVS)



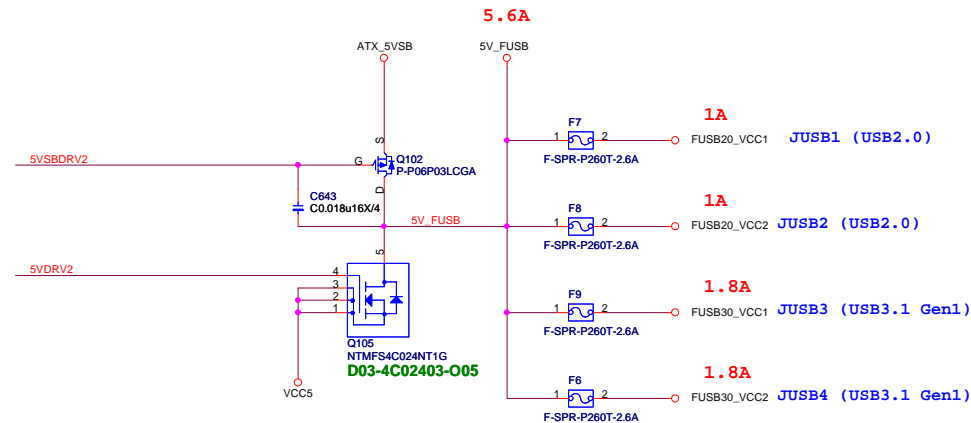
## USB Power



## Rear USB Port Power



## Front USB Port Power

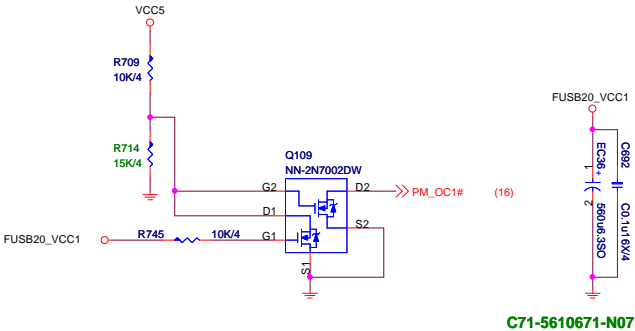
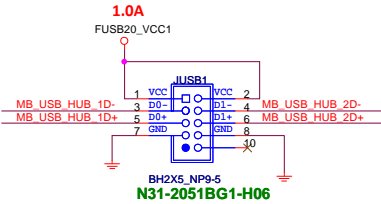
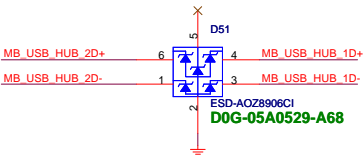
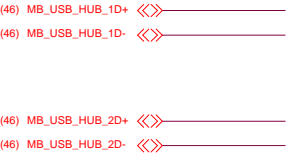


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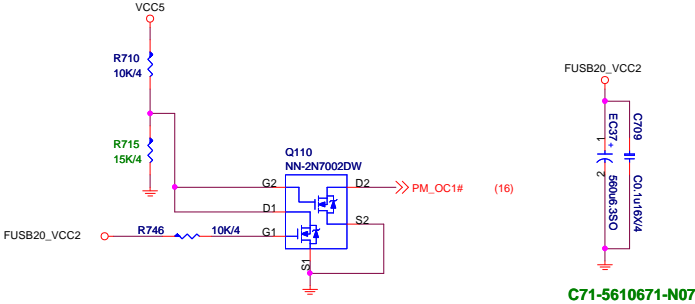
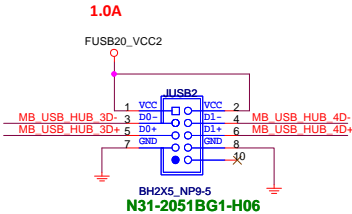
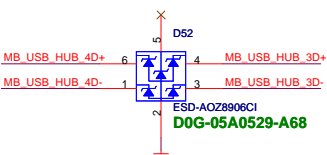
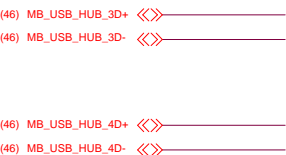
MS-7C37

Size	Document Description	Rev
Custom	USB Power - UP7501	3.0
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Front USB2.0(JUSB1)

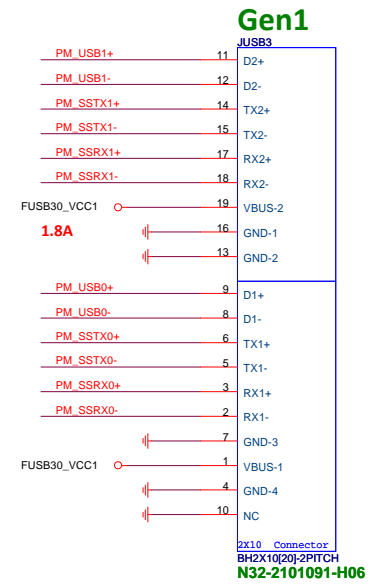
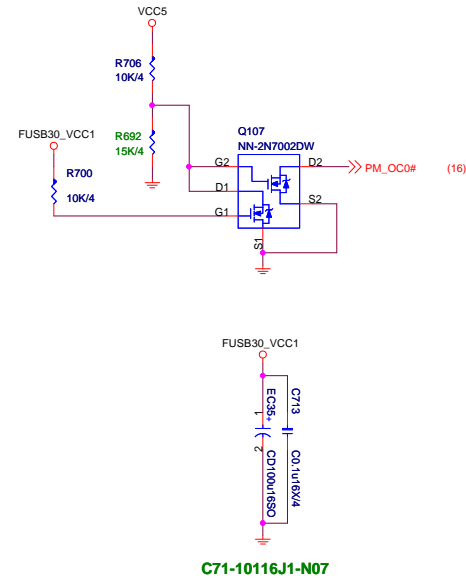
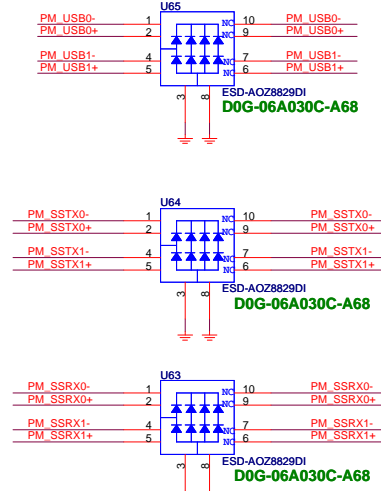
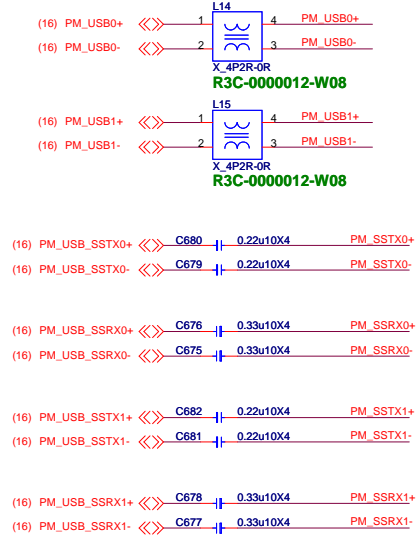


Front USB2.0(JUSB2)

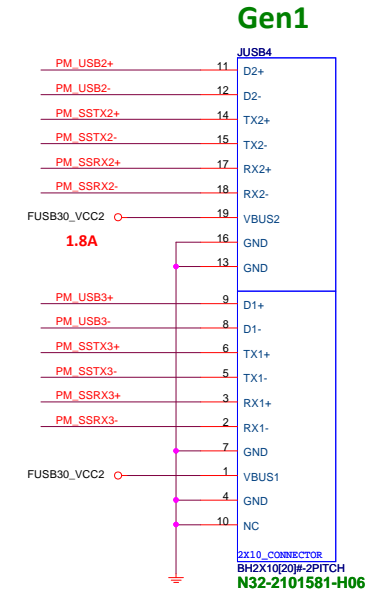
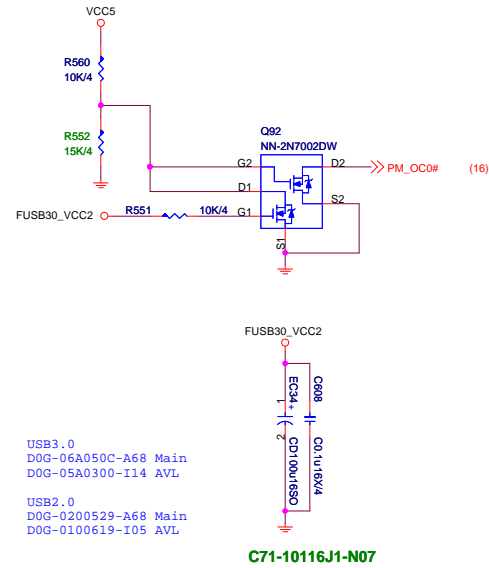
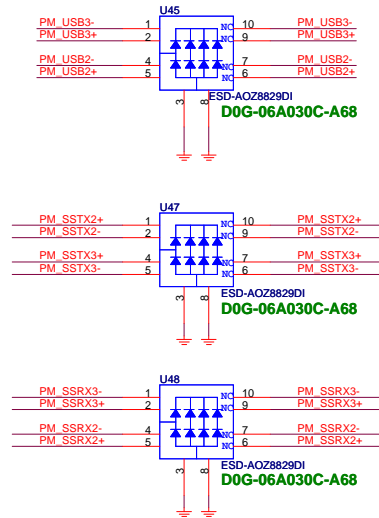
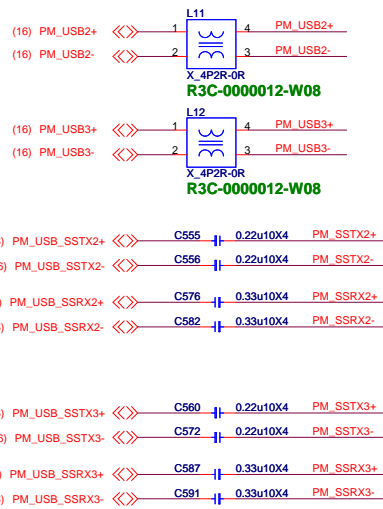




### Front USB3 180° BOX Header(JUSB3)



### Front USB3 90° BOX Header(JUSB4)



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Size Custom	Document Description <b>Front USB3.0 Header</b>	Rev 3.0
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## PS2

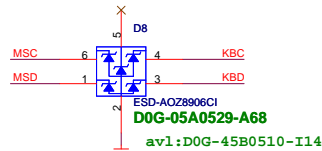
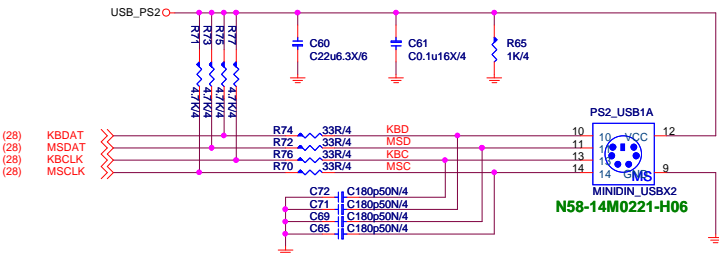
5V@1A

layout note:

C21 must close to TVS pin5

TVS must near KB\_MS1 connector and route without branch

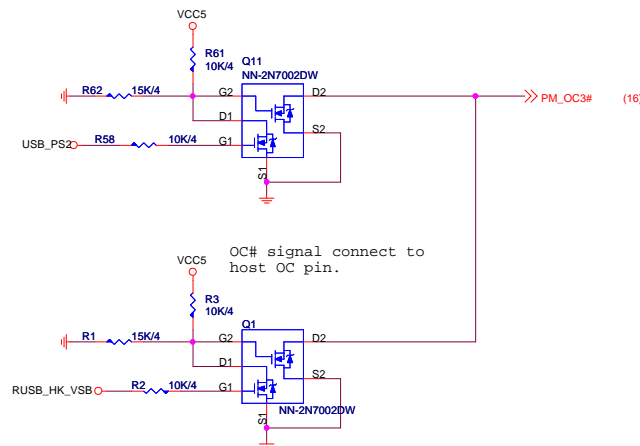
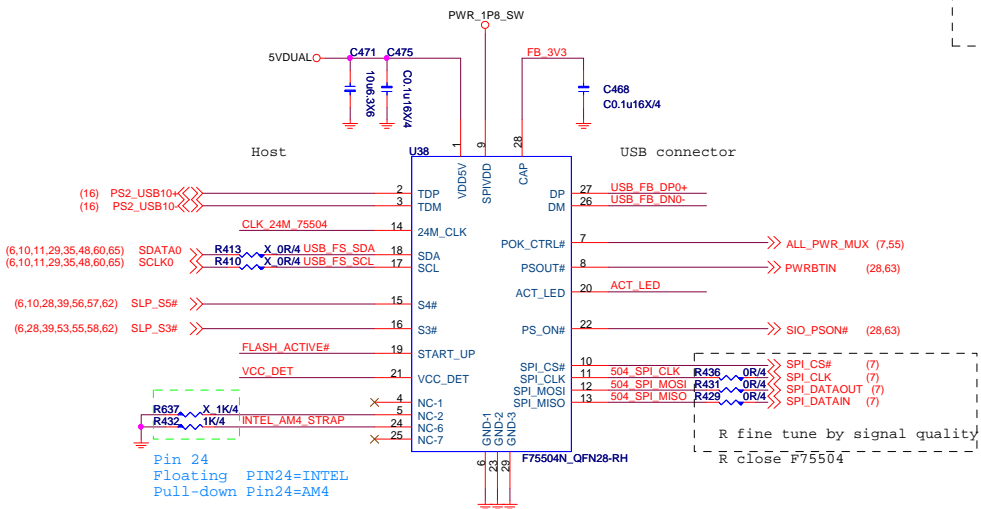
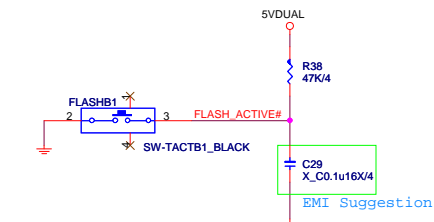
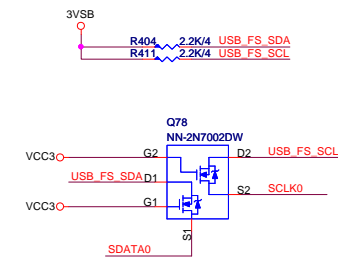
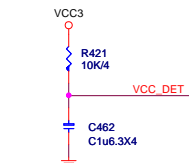
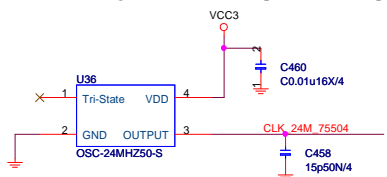
Varistor must close to TVS and route without branch



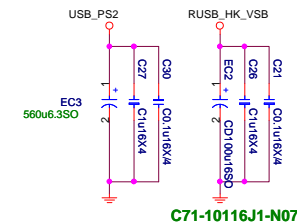
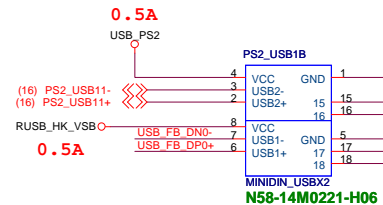
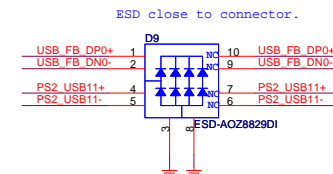
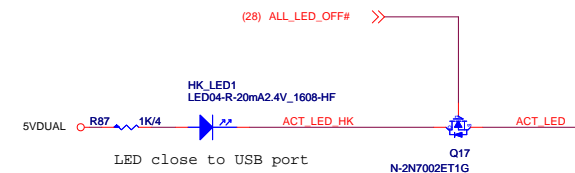
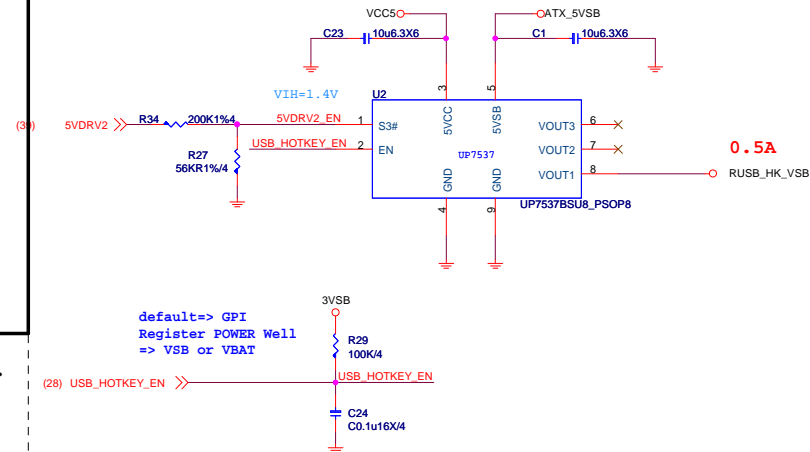
## USB2.0 Flash BIOS

F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.

CLK running in S0,don't require in sleep



## HOTKEY POWER

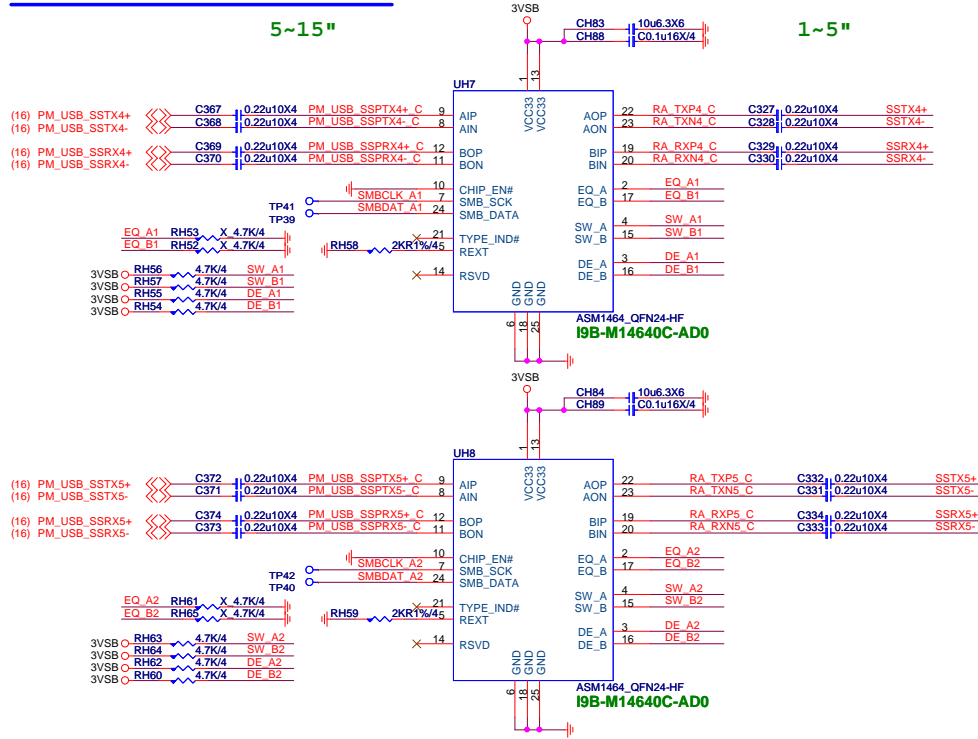


# LAN USB3.1 Gen1 Type-A

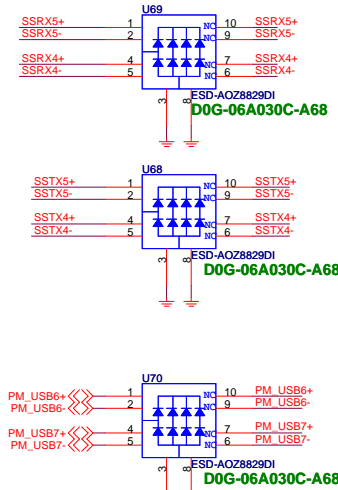
5~15"

0.13A

1~5"

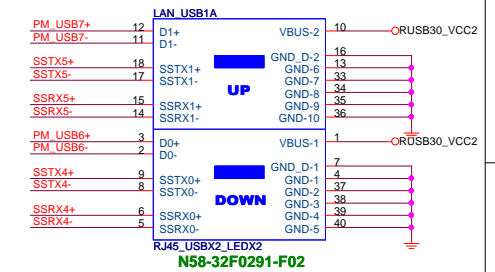


## Rear LAN Type-A

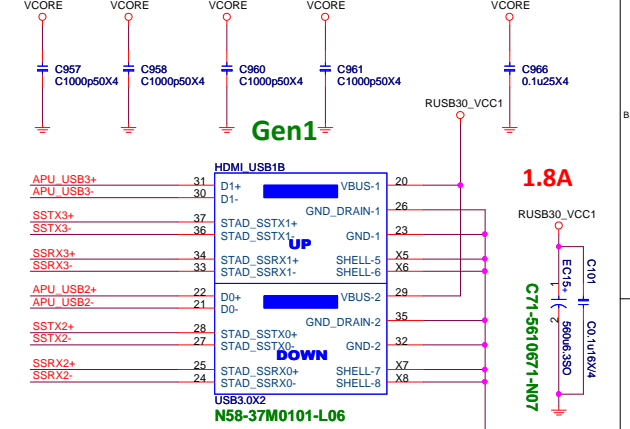
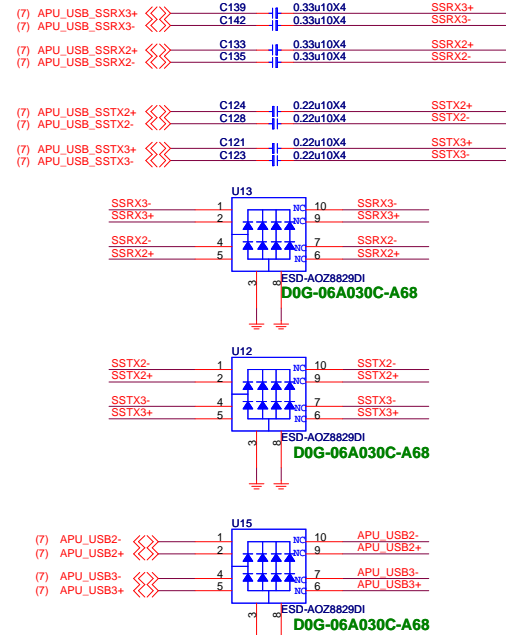
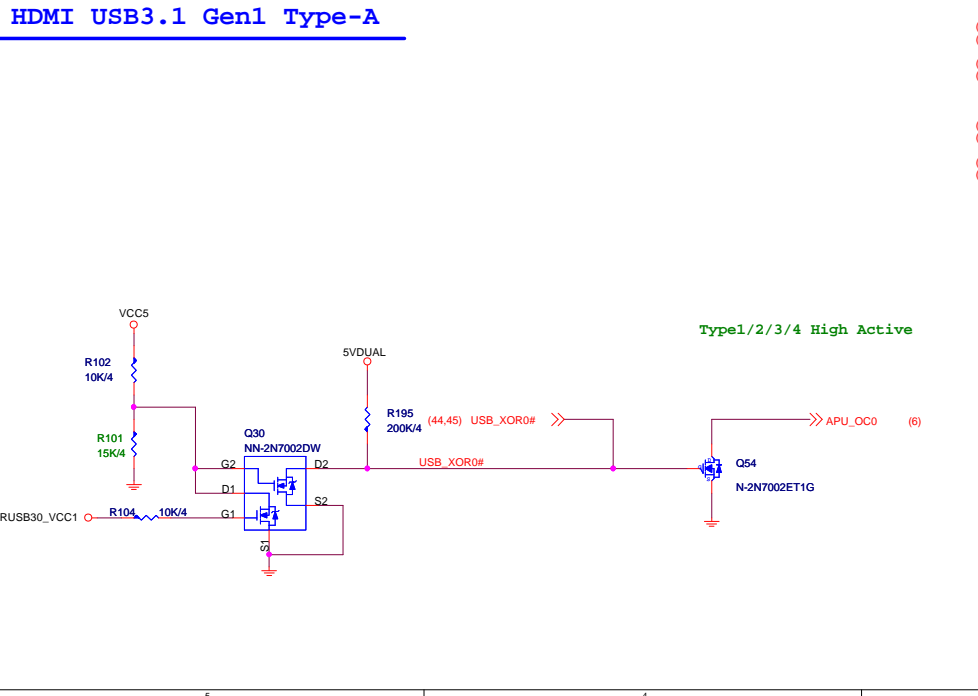


Gen1

1.8A

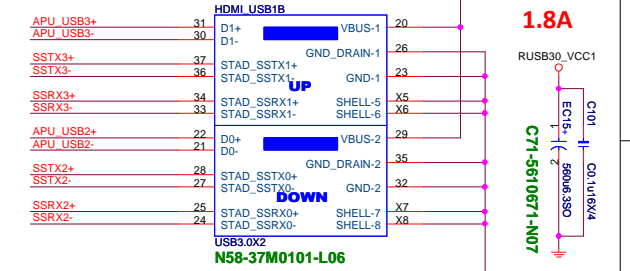


# HDMI USB3.1 Gen1 Type-A

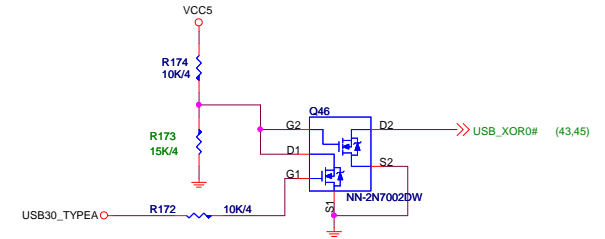
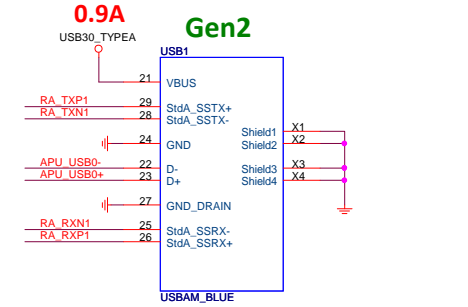
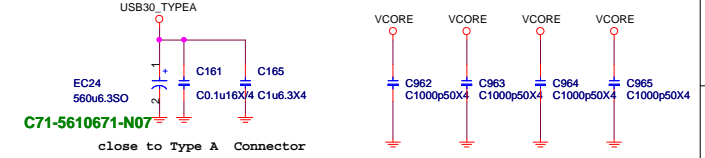
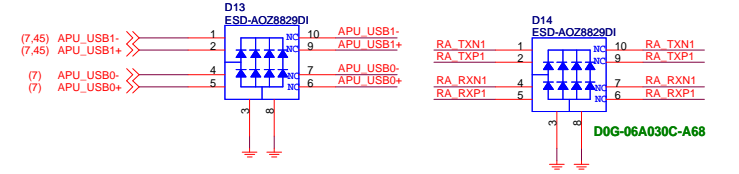
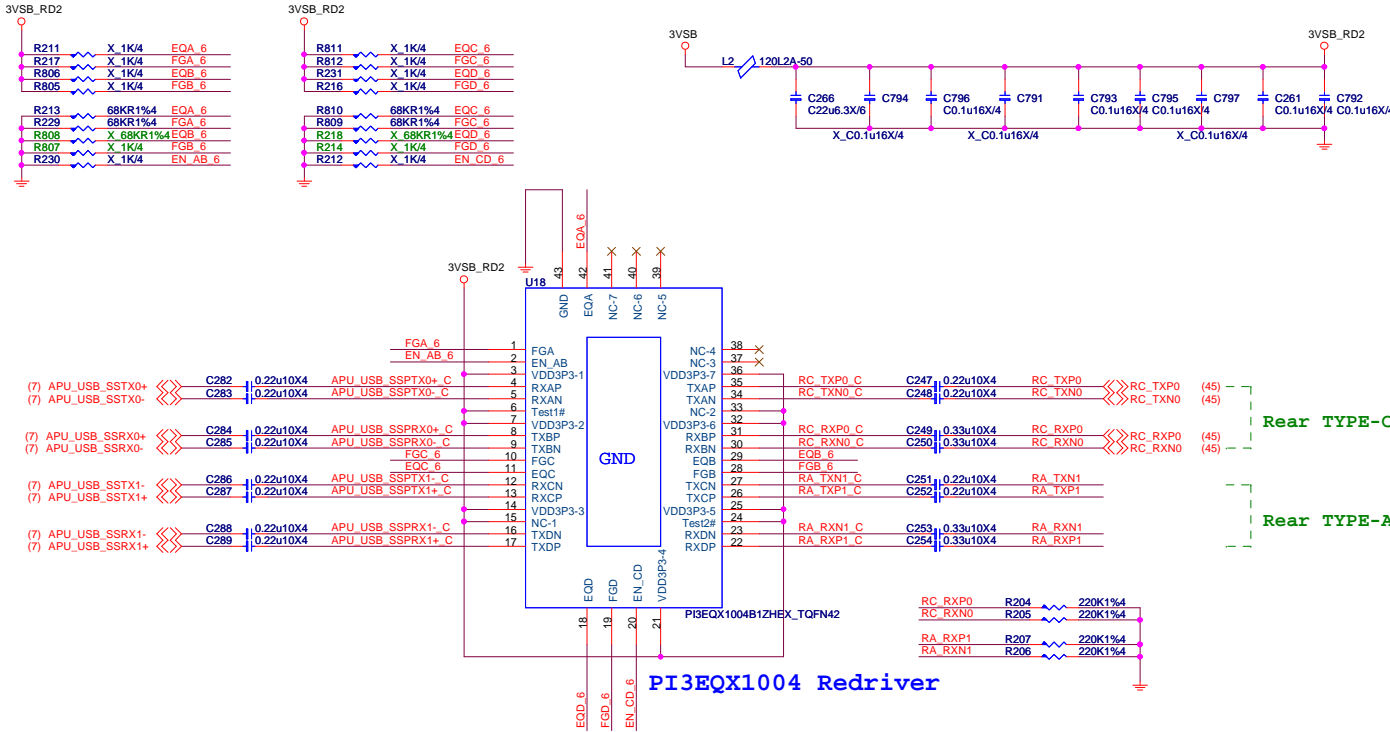


Gen1

1.8A

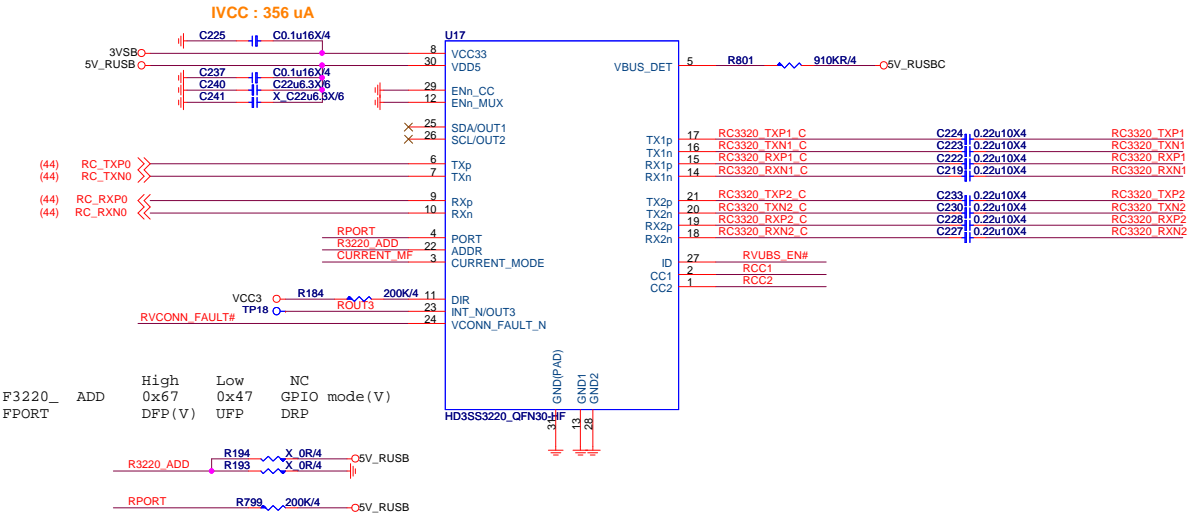


# USB3.1 Gen2 Redriver + Type-A

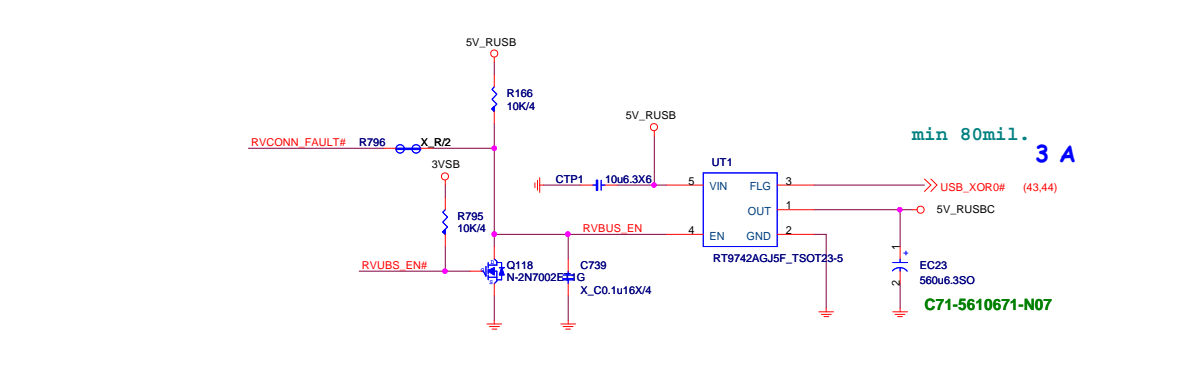


USB3.1 Gen2 Type-C

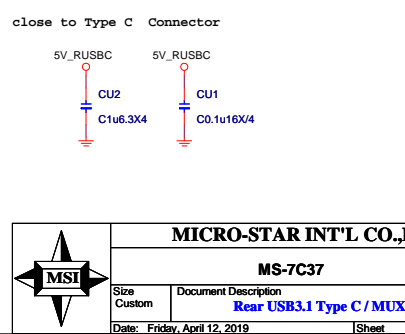
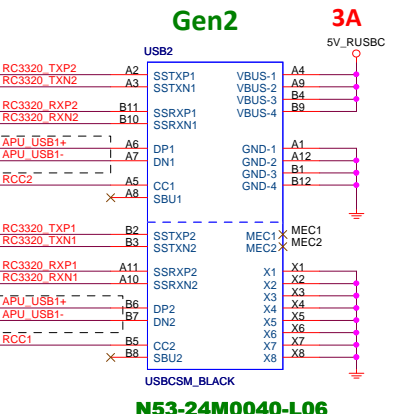
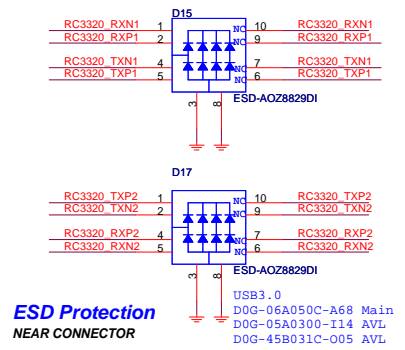
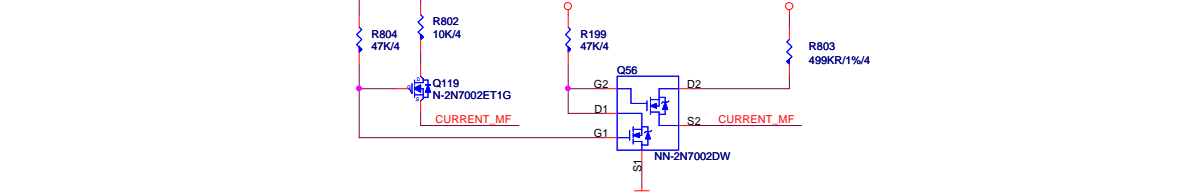
USB Type-C MUX with Configuration Channel (CC)



VBUS EN

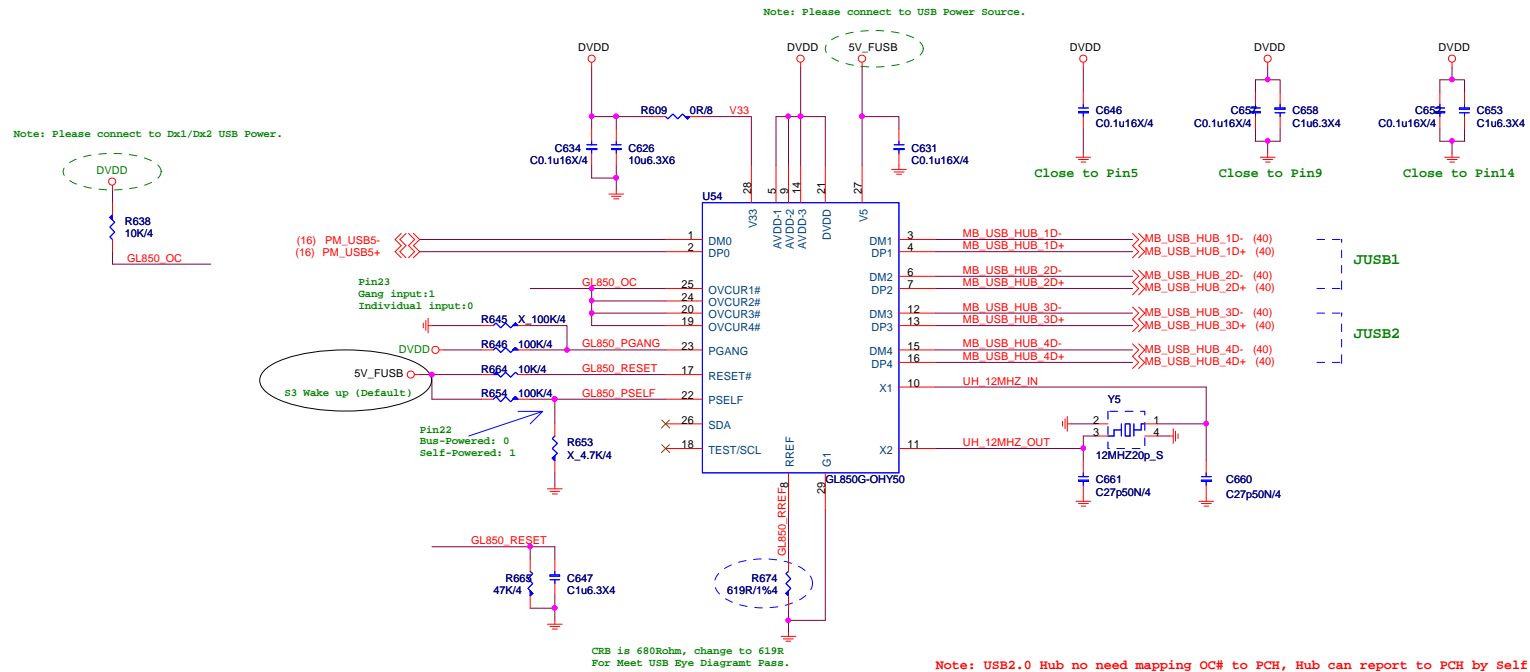


Current Mode



## GL850G USB2.0 HUB

## 5V\_FUSB



**Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.**



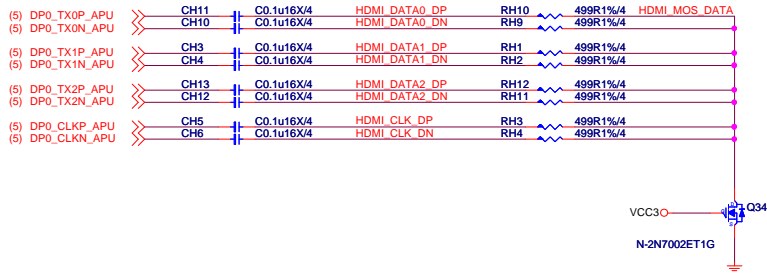
**MICRO-STAR INT'L CO.,LTD**

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# HDMI CONNECTOR

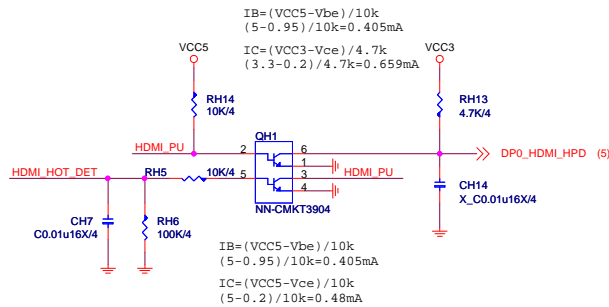
For HDMI 1.4



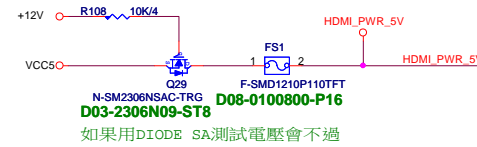
刪除RH6/RH12/RH15/RH16  
For 增加VCC5寬度

For EMI

## HPD Circuit

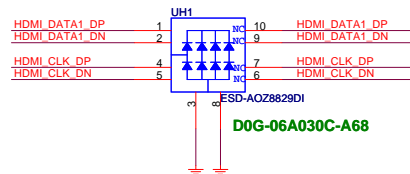
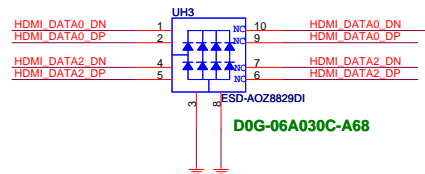


## Connector Power

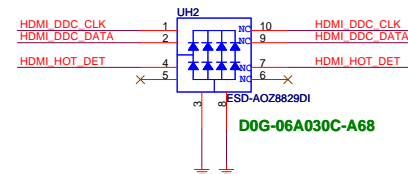


如果用DIODE SA測試電壓會不過

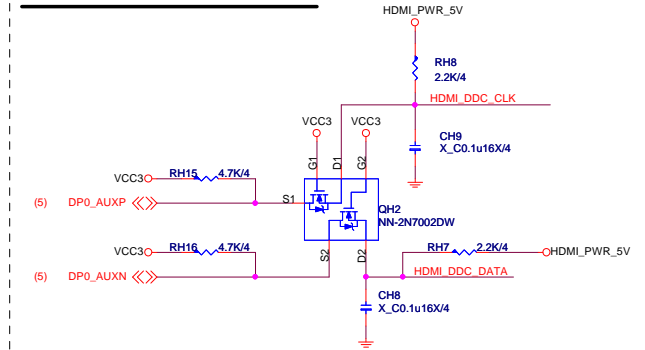
## For EMI



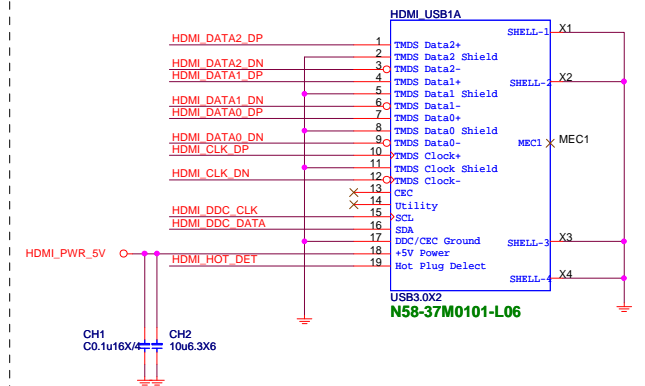
## 注意:耐壓5V零件



## AUX Level Shifter



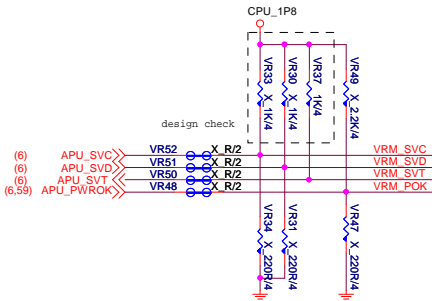
## Connector



MICRO-STAR INT'L CO.,LTD

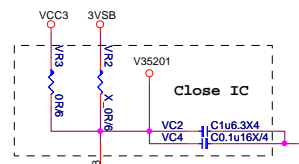
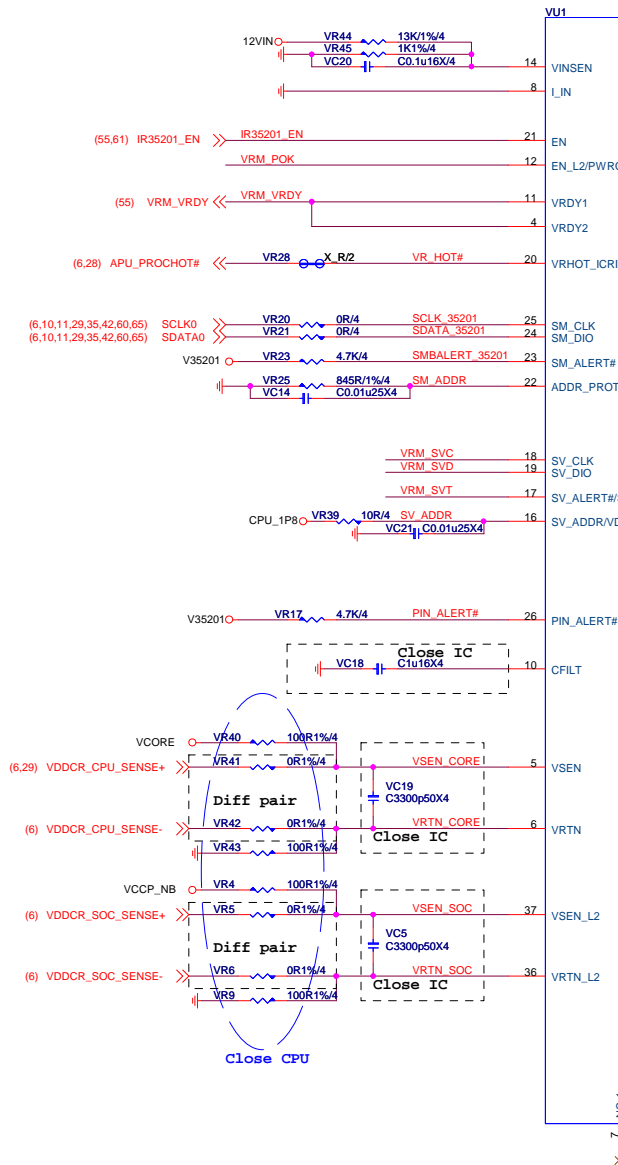
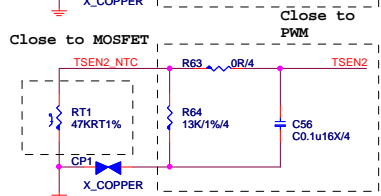
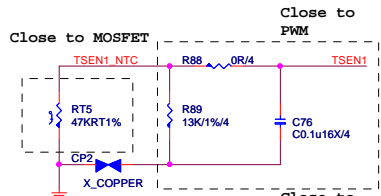
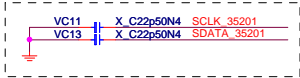
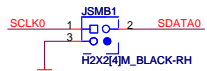
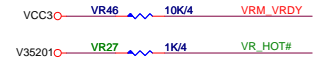
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Custom	HDMI	3.0
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Note:VID Override Circuit

BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



燒錄打點:IC正面上橋+金色點



VCORE: ICCMax 140A  
LL: 1.3mohm  
OCP: 192A  
SOC: ICCMax 75A  
LL: 2.1ohm  
OCP: 90A

Phase 1 close to CPU power pin.

RT close to Choke

RT close to Choke

0x26:RH=18K,RL=13K							
Default	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X



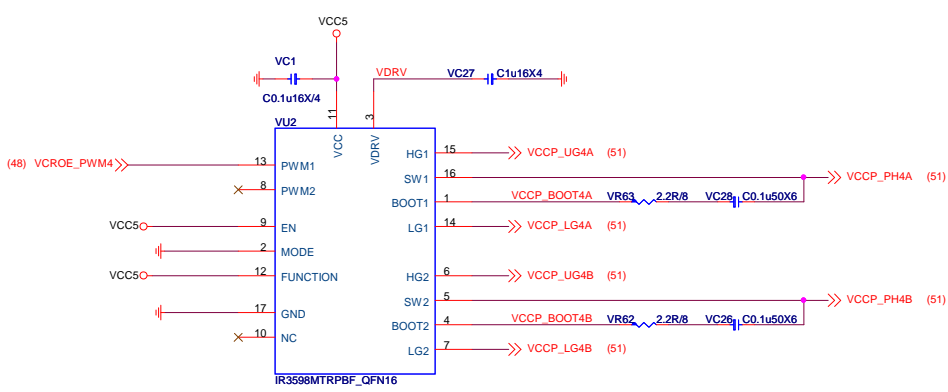
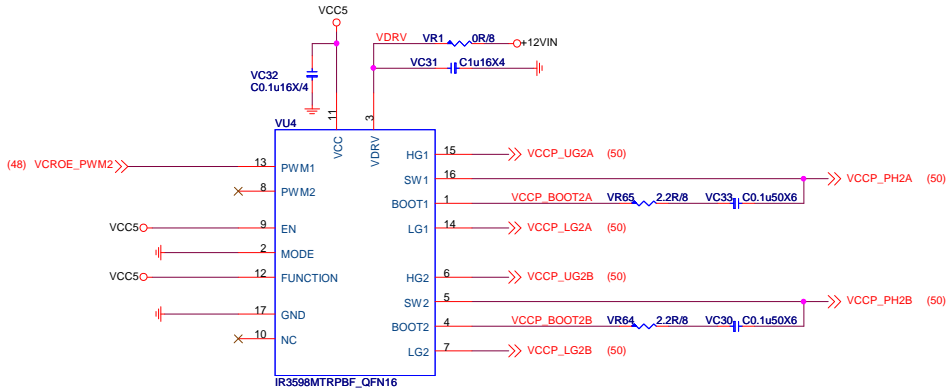
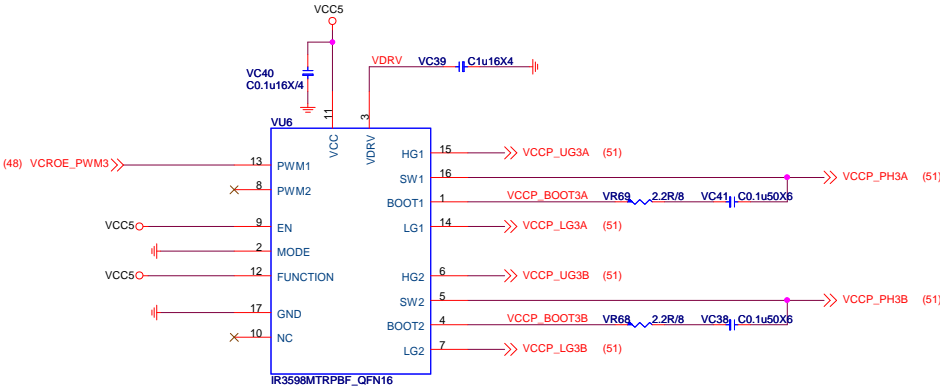
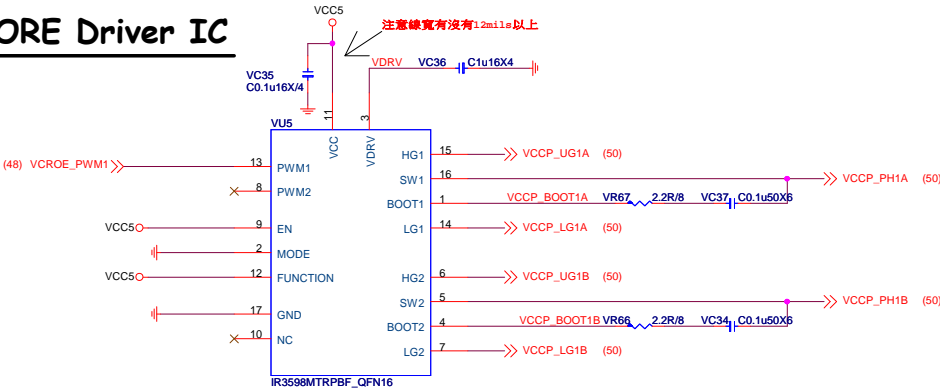
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power IR35201 8+2	3.0
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CPU\_CORE Driver IC



CPU\_SOC Driver IC

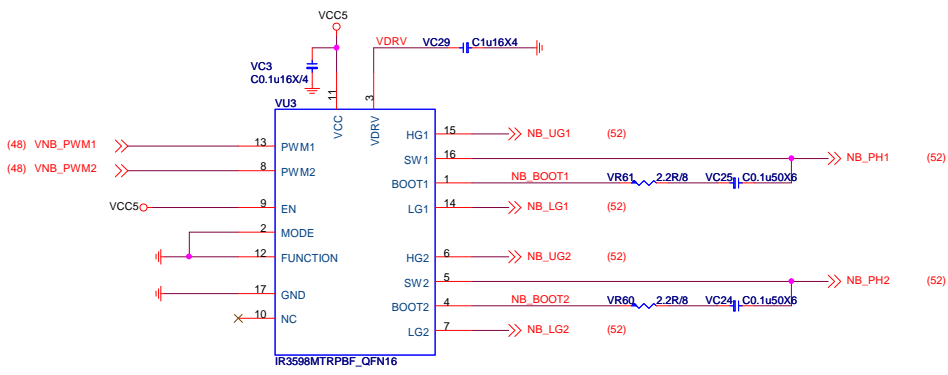


Table for IR3598

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler

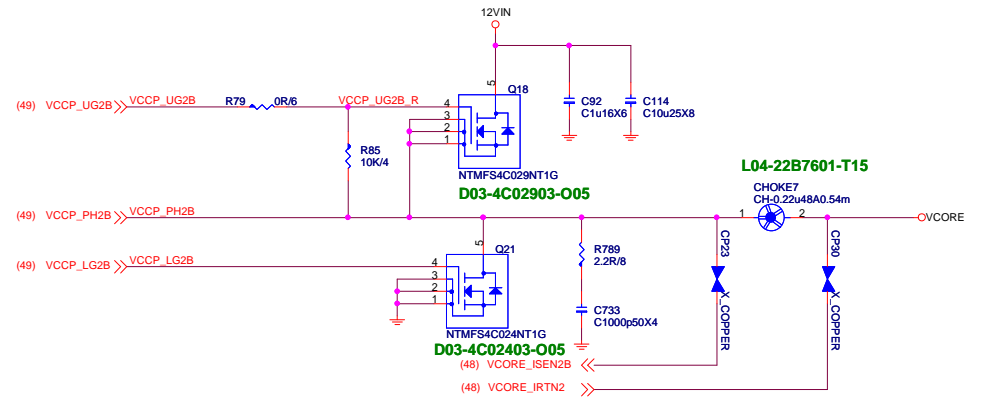
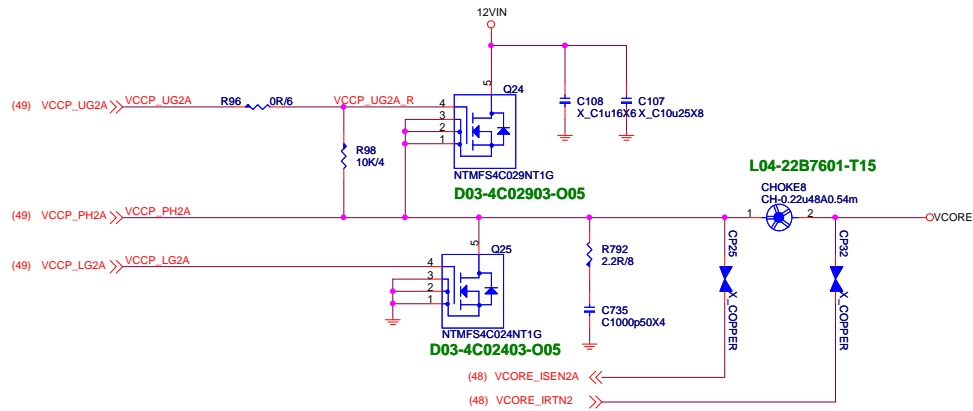
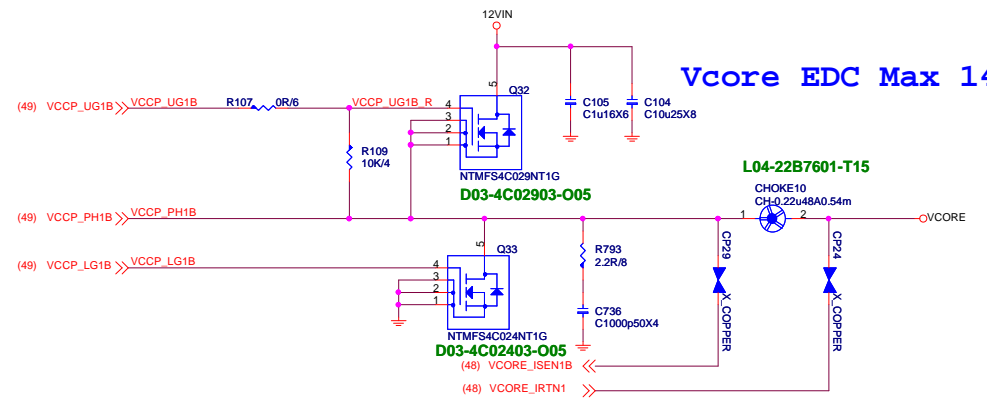
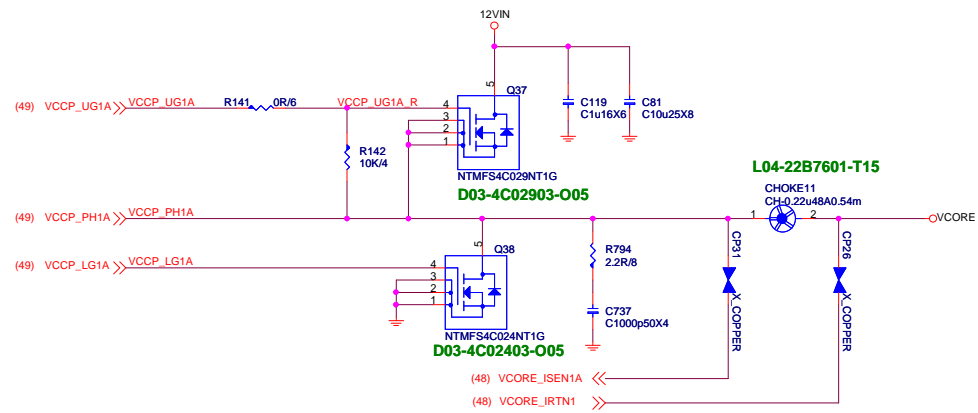
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore

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Size Custom Document Description **CPU Power Driver IC IR3598** Rev 3.0

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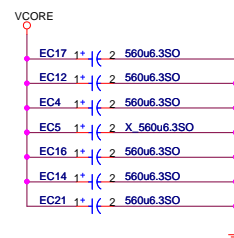
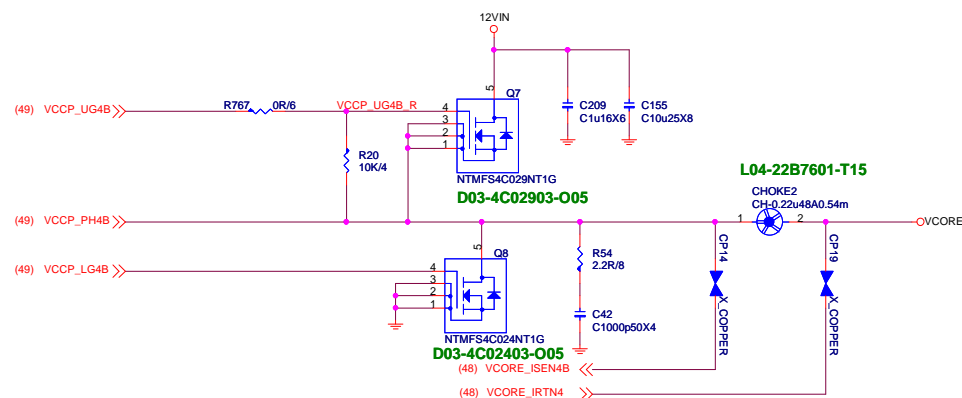
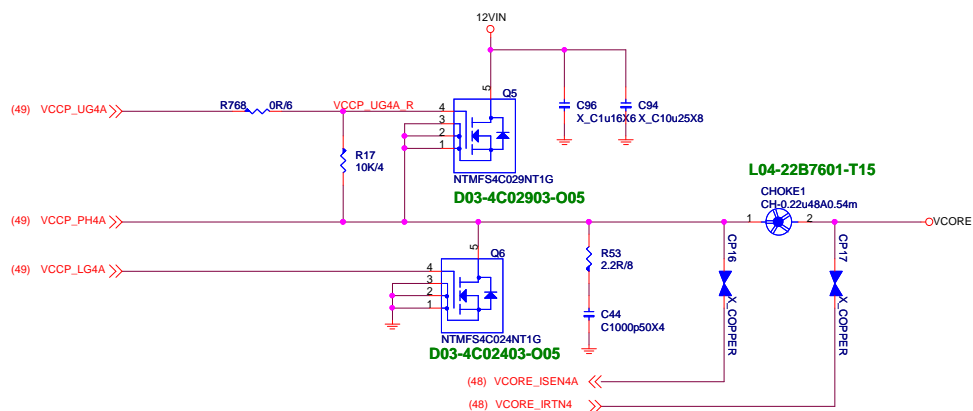
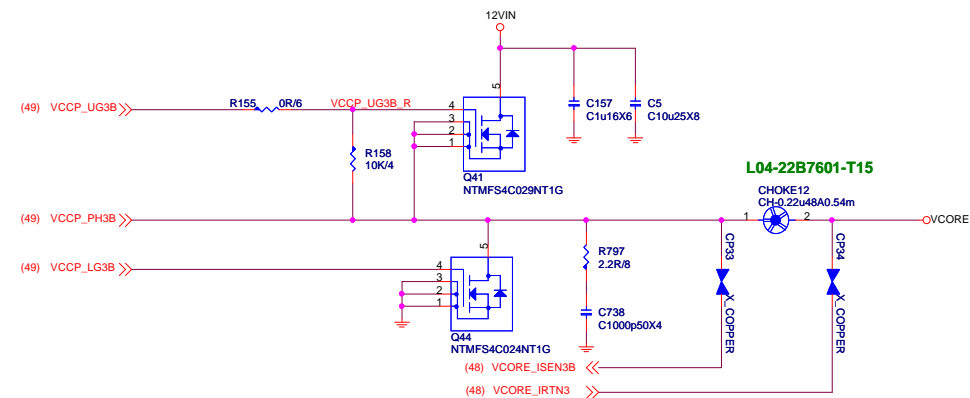
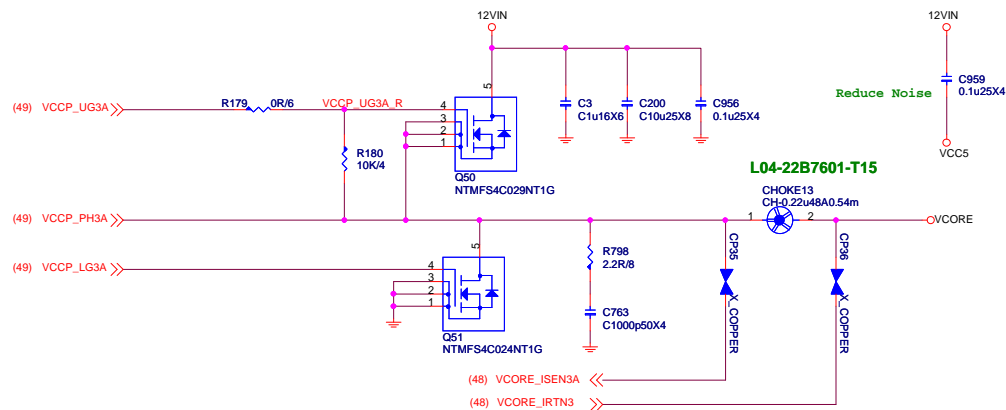
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD

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Custom	CPU Power Vcore Phase 1-6	3.0
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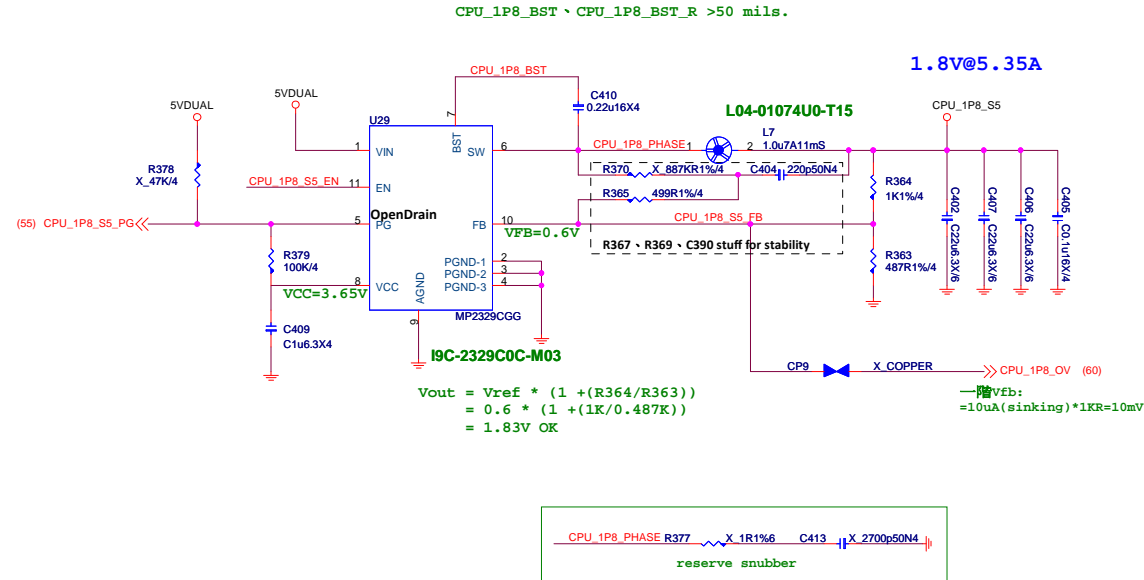
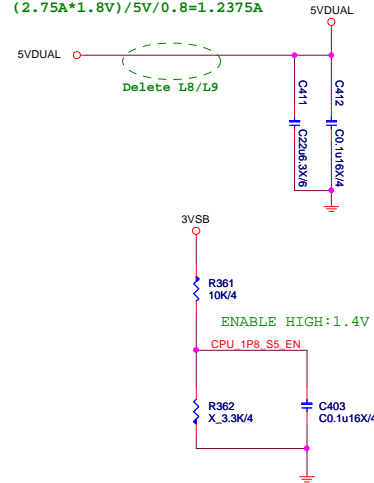


## CPU\_1P8V\_S5

CPU: VDD\_18\_S5@0.5A  
CPU: VDDIO\_Audio@0.25A  
CHIP: VDD\_18\_S5@0.1A

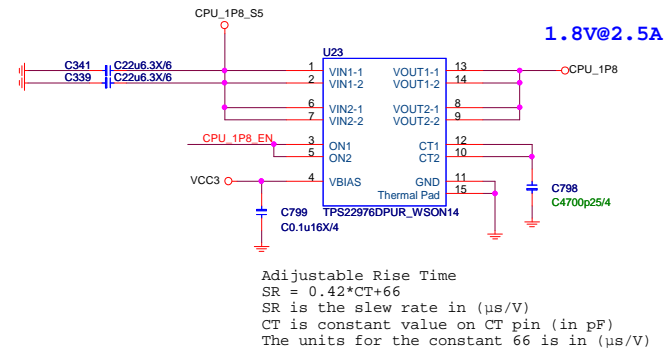
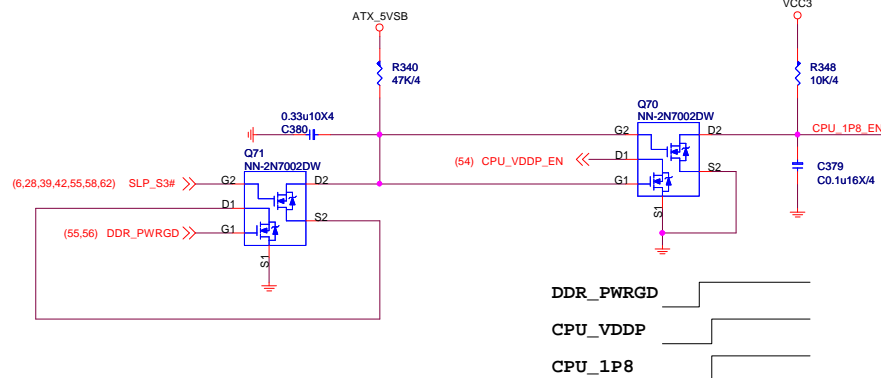
CPU\_1P8: 2.5A  
CPU\_VDDP\_S5: 1A  
CHIP\_SOC\_S5: 1A

Input Current=  
(2.75A\*1.8V)/5V/0.8=1.2375A



## CPU\_1P8V

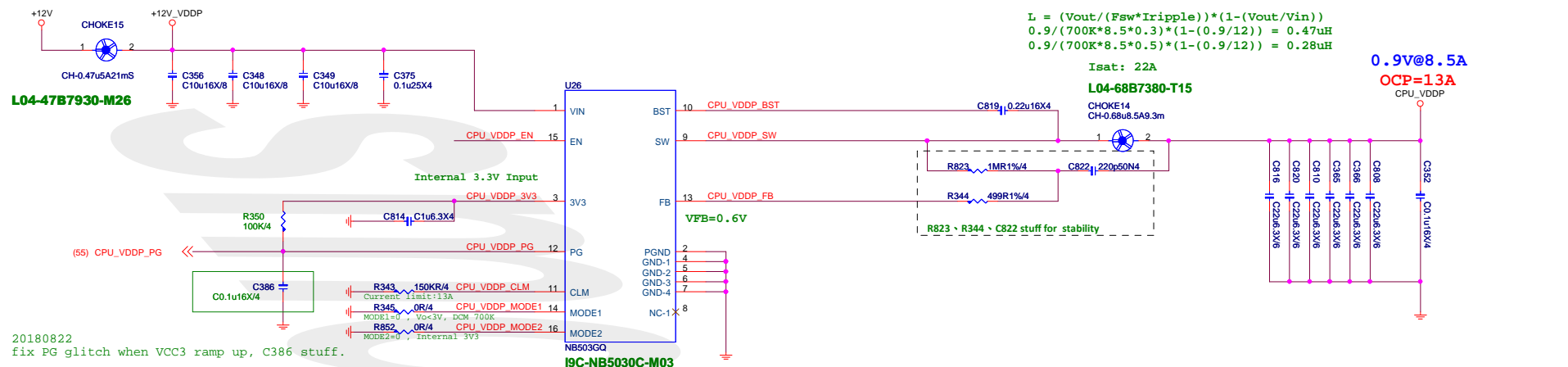
CPU: VDD\_18@2A  
CHIP: VDD\_18@0.5A



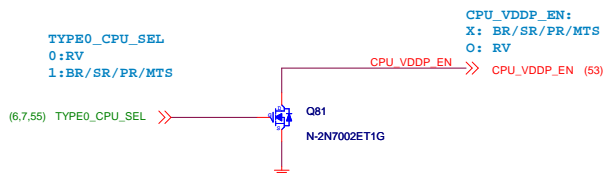
Adjustable Rise Time  
 $SR = 0.42 \times CT + 66$   
SR is the slew rate in ( $\mu s/V$ )  
CT is constant value on CT pin (in pF)  
The units for the constant 66 is in ( $\mu s/V$ )


## CPU: VDDP@8.5A

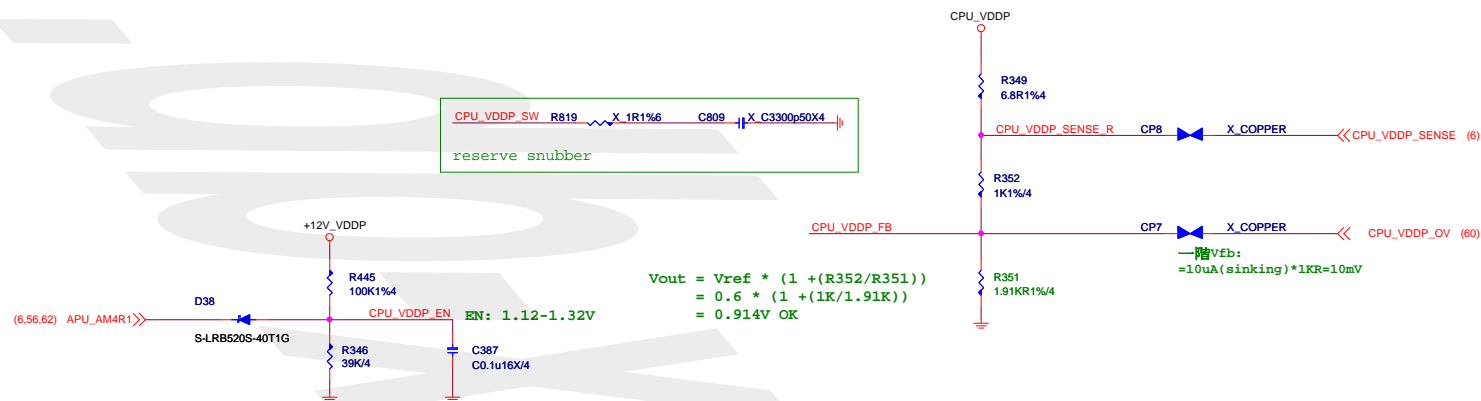
```
Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```



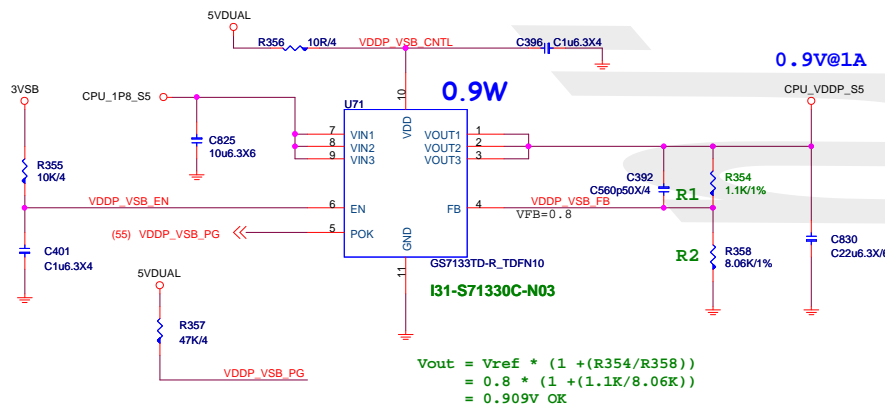
## No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC no1 Support
NA		0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	
RV/ ZP	3	0	1	1
MTS	4	1	CPU VDDP NOT SUPPORT TYHE4	



## CPU: VDDP S5@1A



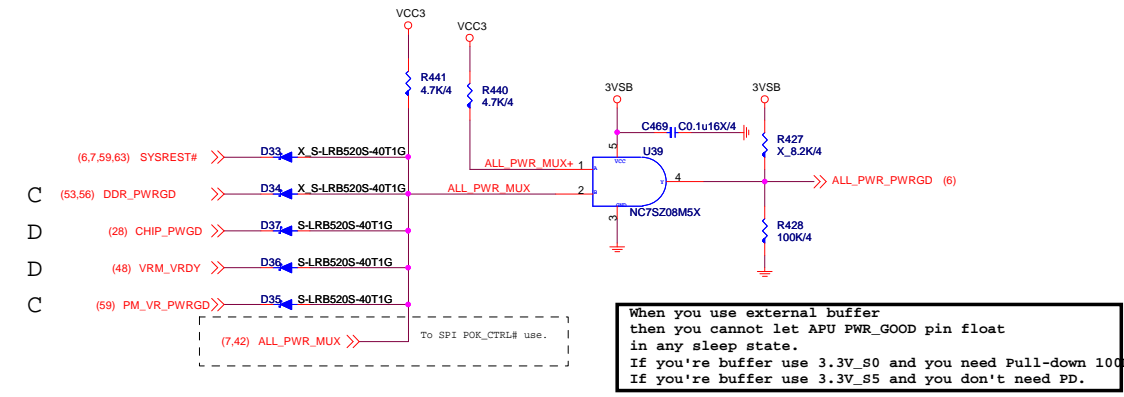
**MICRO-STAR INT'L CO.,LTD**

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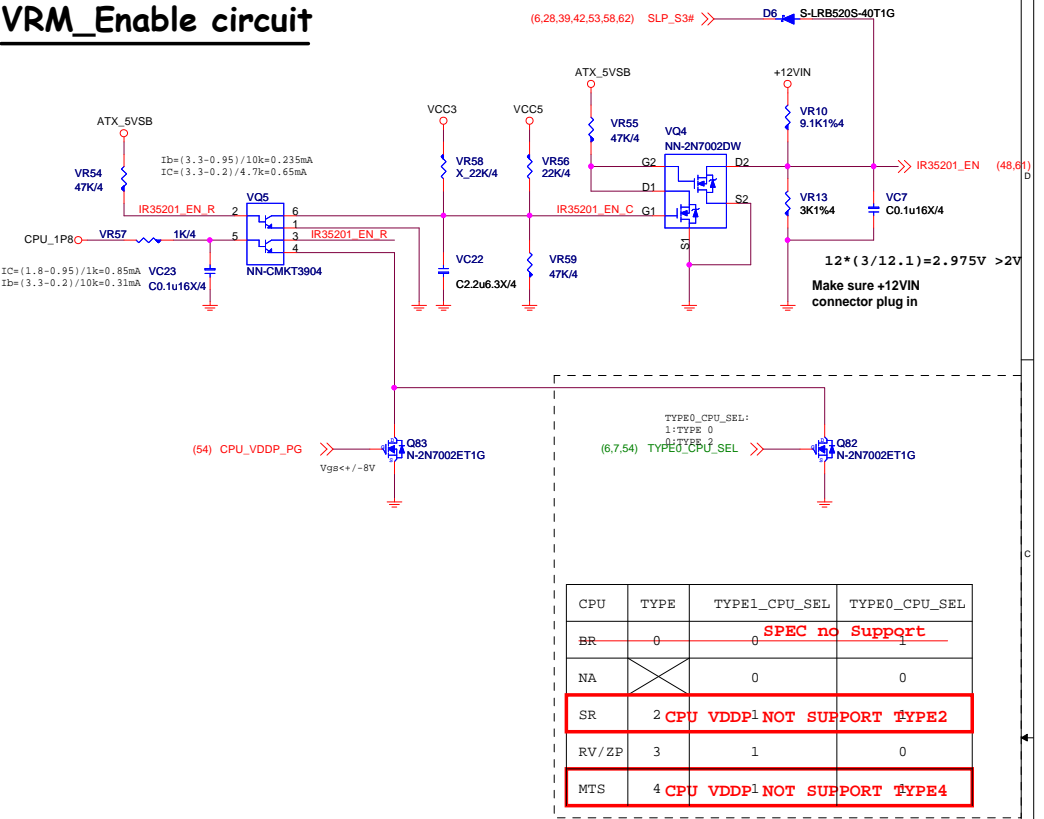
Size Custom	Document Description <b>CPU Power VDDP - NB503</b>	Rev 3.0
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ALL POWER GOOD MUX

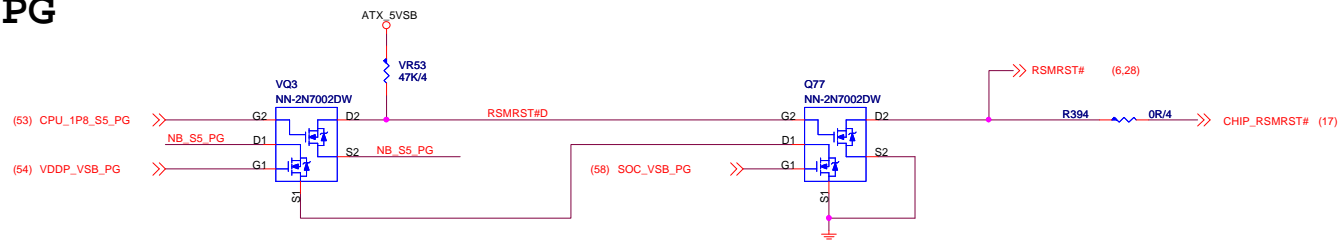
S0 PG



VRM\_Enable circuit



S5 PG



15.5A For CPU  
9.5A For 4DIMM  
1.2A For DDR VTT

### 15.5A For CPU

### 9.5A For 4DIMM

### 1.2A For DDR VTT

OCP = 39.3A; Choke Isat=42A

$$R_{ocset} = 1.5 * I_{max} * R_{dson(low)} / I_{ocset}$$

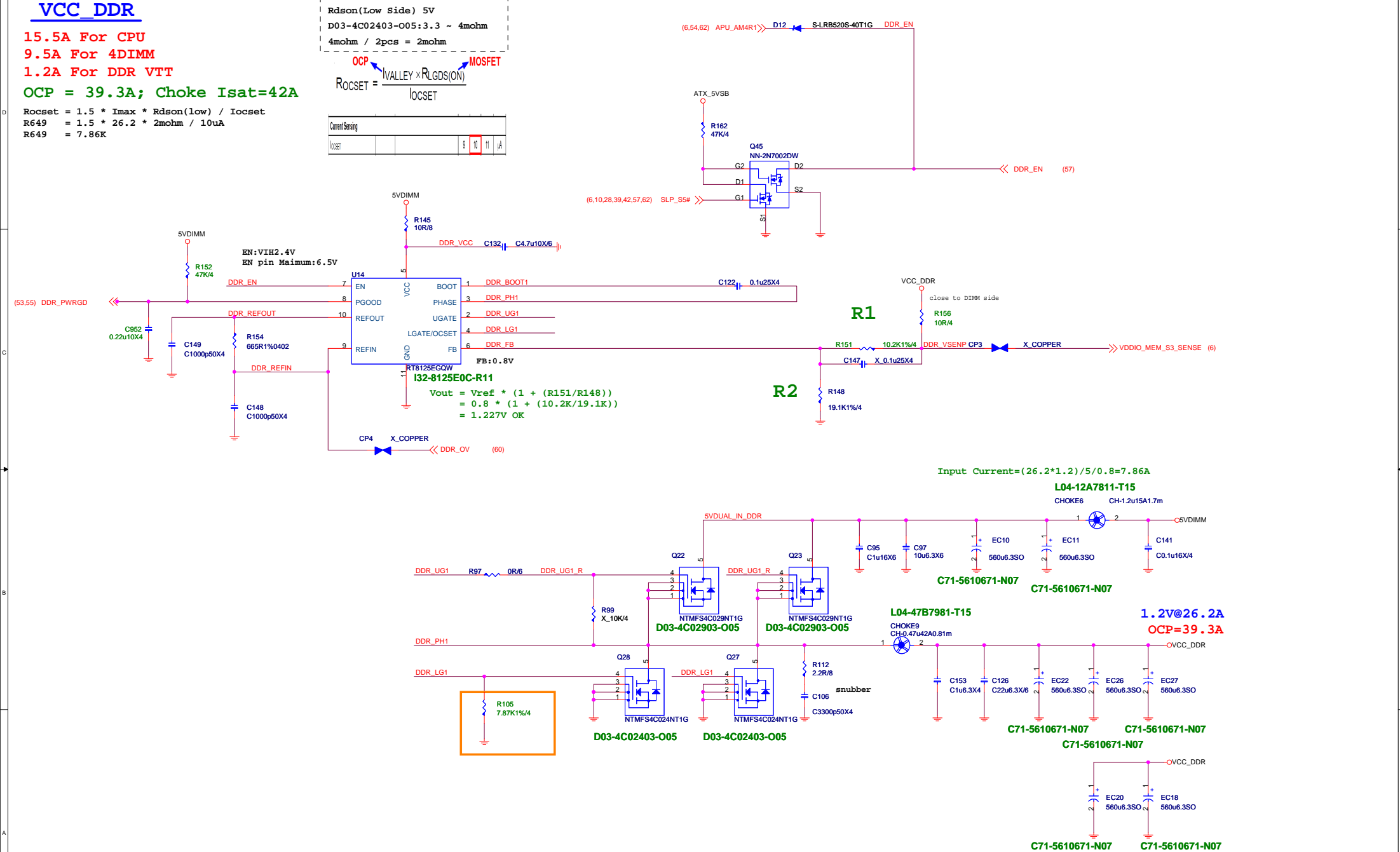
```
R649    = 1.5 * 26.2 * 2mohm / 10uA
```

R649 = 7.86K

Rdson(Low Side) 5V  
D03-4C02403-O05:3.3 ~ 4mohm  
4mohm / 2pcs = 2mohm

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Current Sensing				
ioset		9	10	11 $\mu A$



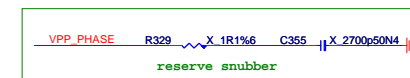
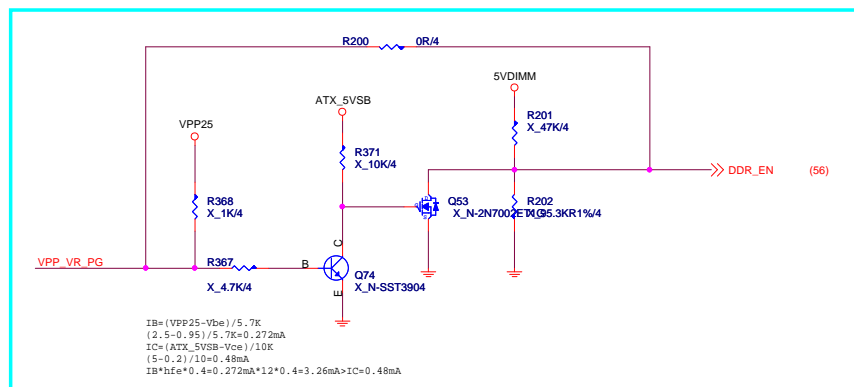
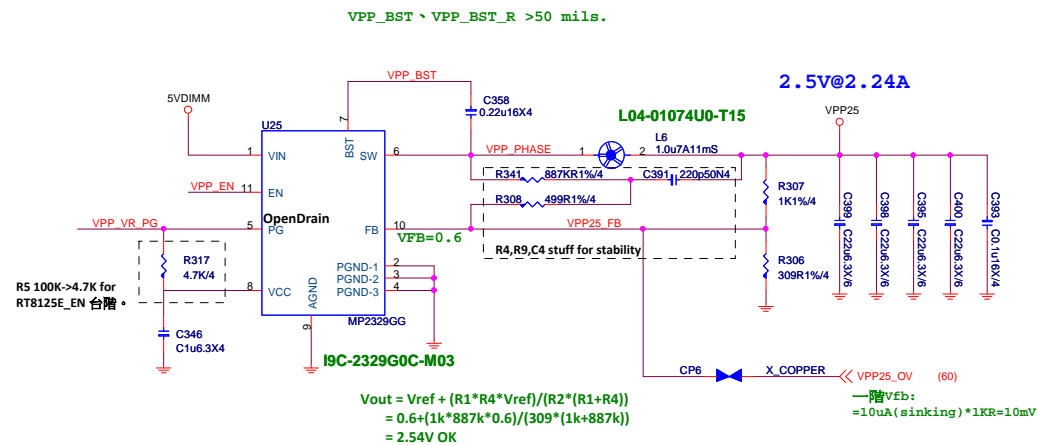
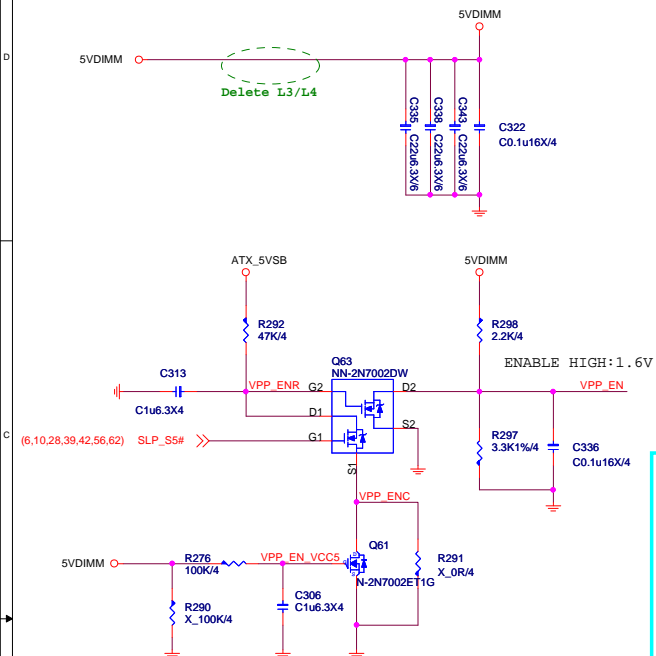
**MICRO-STAR INT'L CO.,LTD**

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Size Custom	Document Description <b>DDR Power - 8125E</b>	Rev 3.0
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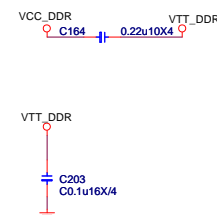
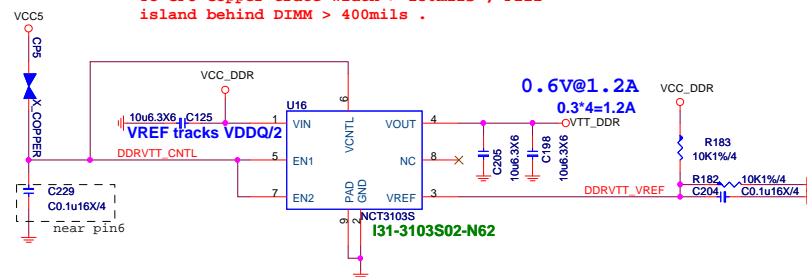


## 2.5V@2.24A



0.6V@1.2A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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Size Custom	Document Description <b>DDR VPP25 / VTT</b>
----------------	------------------------------------------------

Rev	3.0
-----	-----

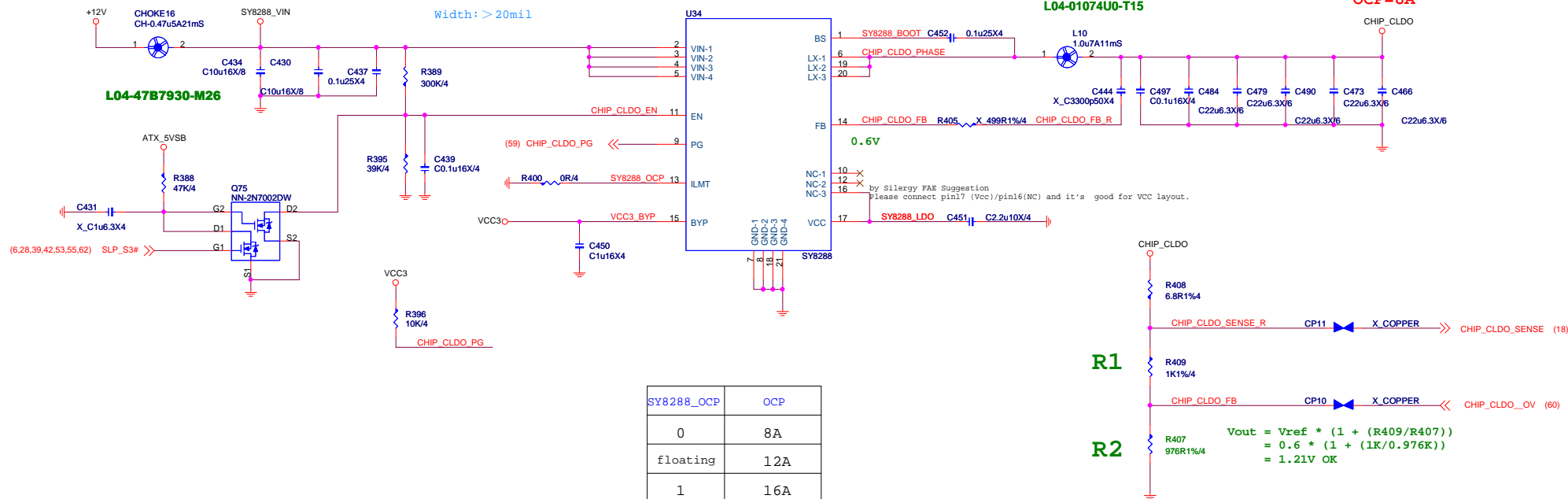
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# CHIP\_CLDO

CHIP: VDD\_CLDO@5A

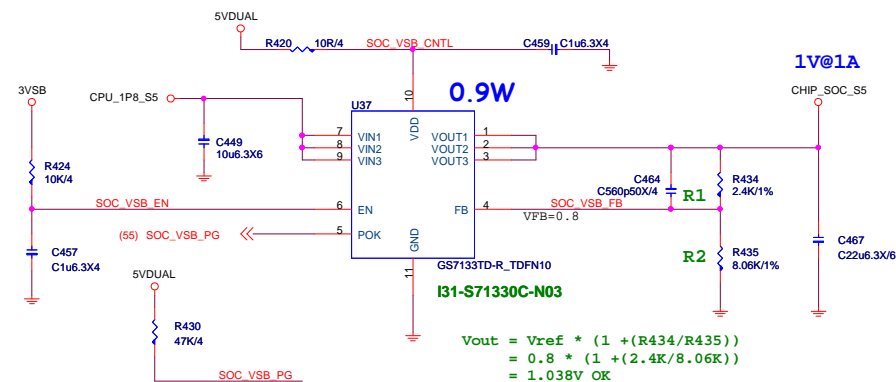
Input Current= (5.5A\*1.05V)/12V/0.8=0.625A

1.2V@5A  
OCP=8A



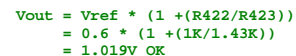
# CHIP\_SOC\_S5

CHIP: VDDCR\_SOC\_S5@1A



## CHIP: VDDCR\_SOC@9A

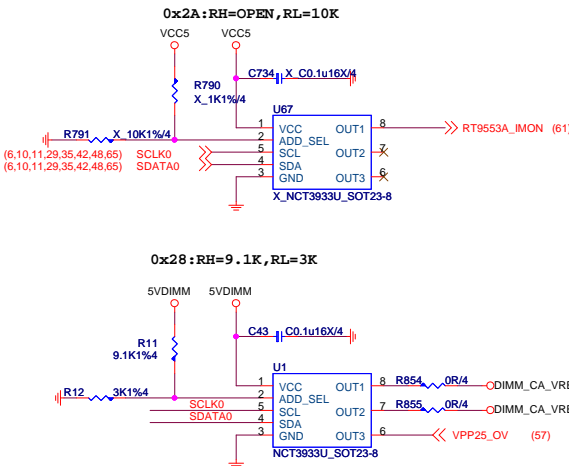
```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH
```



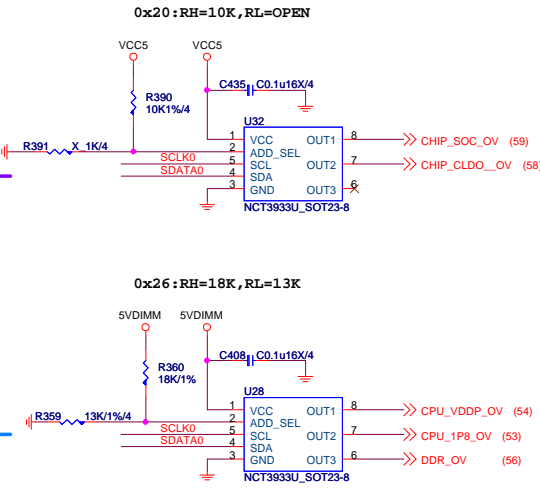
MS-7C37

Size Custom	Document Description <b>PROM - NB503 / 1.0V</b>	Rev 3.0
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Over Voltage Control IC



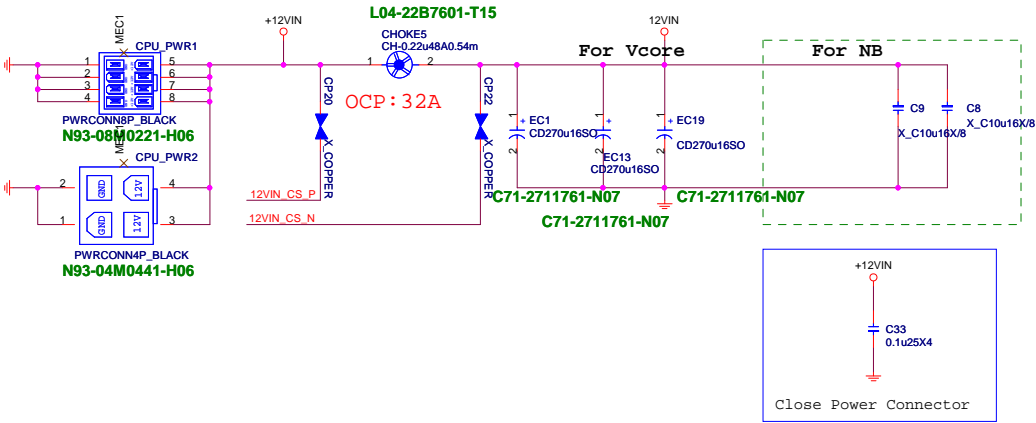
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

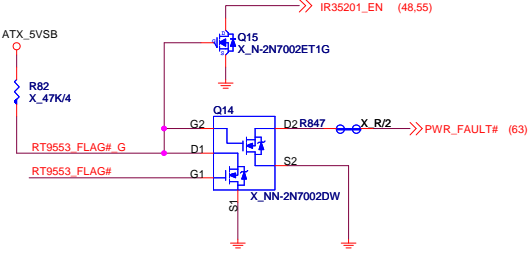
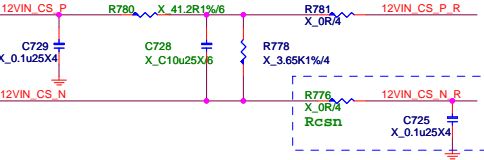
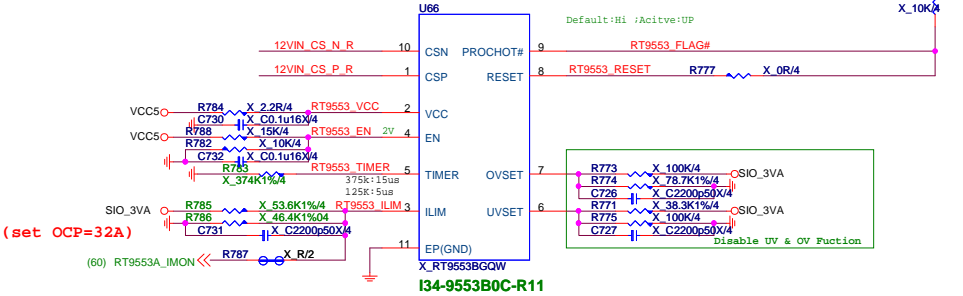
CPU POWER CONNECTOR



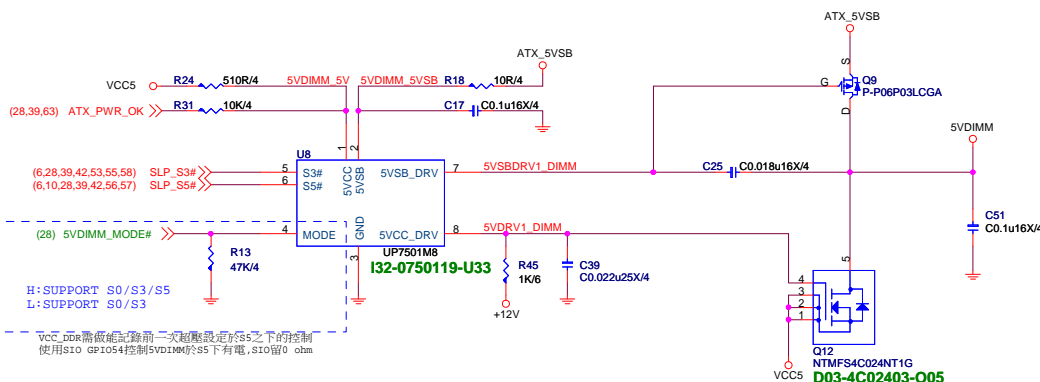
Vcore		SOC	
$D = V_{out}/V_{in}$		$D = V_{out}/V_{in}$	
$V_{in} = 12$	> input voltage	$V_{in} = 12$	> input voltage
$V_{out} = 2$	> output Vcore	$V_{out} = 1.55$	> output Vcore
$D = 0.166667$		$D = 0.129167$	
$I_o = I_{core(max)} * 0.8$		$I_o = I_{core(max)} * 0.8$	
$I_{core(max)} = 200$	> Vcore current	$I_{core(max)} = 75$	> Vcore current
$I_{avg} = 160$	A	$I_{avg} = 60$	A
$I_{ripple} = \{ I_o * \sqrt{D * \sqrt{(1-D)}} \} / \text{Phase}$		$I_{ripple} = \{ I_o * \sqrt{D * \sqrt{(1-D)}} \} / \text{Phase}$	
Phase = 10	phase	Phase = 2	phase
$I_{ripple} = 5.962848$	A	$I_{ripple} = 10.06153$	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
$I_{ripple(cap)} = 4700$	m A	$I_{ripple(cap)} = 4700$	m A
$COE_{TEMP} = 1$		$COE_{TEMP} = 1$	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



## 5VDIMM FOR DDR



## 3VSB cost down

3.3V@3.363A

CPU: VDD\_33\_S5@0.25A

CHIP: VDD\_33\_S5@0.1A

PCIE\*4@1.5A

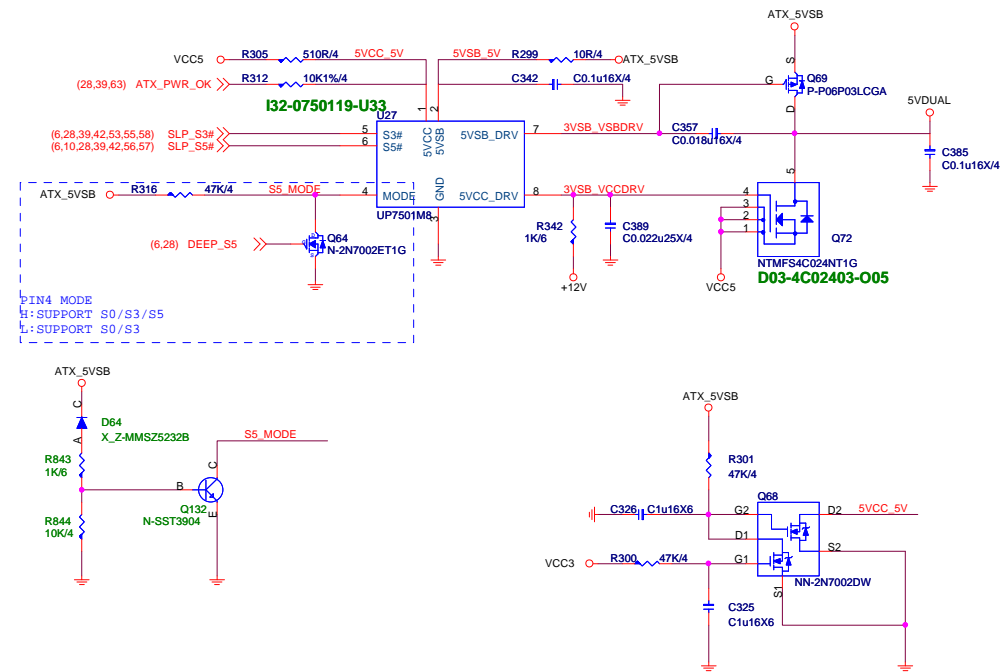
M.2\_WIFI@0.78A

LAN@0.065A

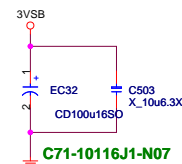
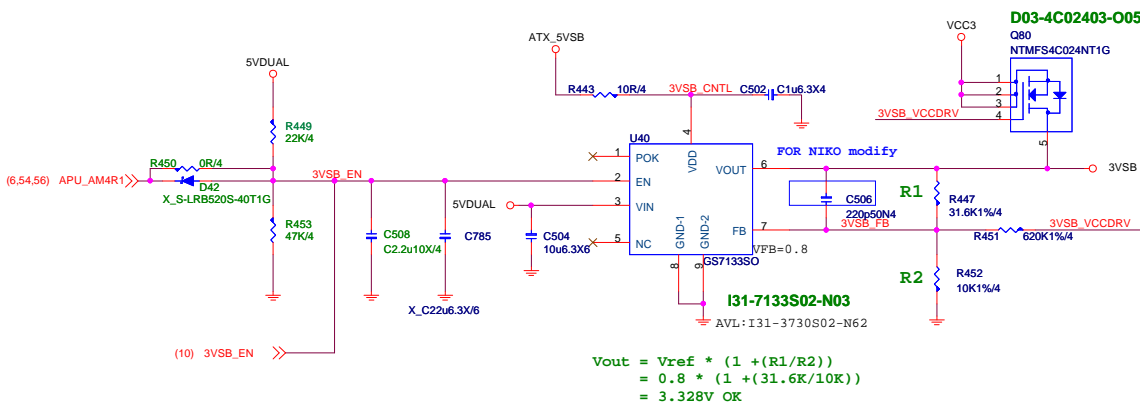
Redriver\*2@0.668A

USB TYPE-C@0.9mA

## 5VDUAL For 3VSB、CPU 1.8V、VDDP

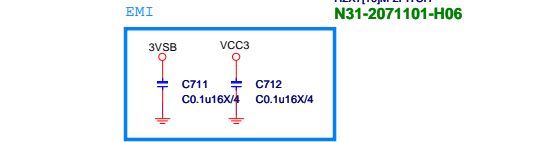


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VSDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VSDRV1 delay 6ms assert), but VCC3 not ready and let the 3VSB sequence fail.



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Custom	ACPI - 3VSB / 5VDIMM		3.0
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**TPM**



PWSW+ C714 X\_C0.1u16X/4

[illegible]

VCORE ○ — F\_check VTC1

VCCP\_NB ○ — F\_check VTC2

CPU\_VDDP ○ — F\_check VTC4

VCC\_DDR ○ — F\_check VTC3

CPU\_1P8 ○ — F\_check VTC5

VBAT ○ — F\_check VTC6

Put Bottom Side

**FRONT PANNEL**

VCC5

R760 330R/4

HDD+ 1

IDE\_LED 3

C715 X C0.1u16X/4

R764 33R/4

C724 C0.1u16X/4

JFP1

HDD+ 1

IDE\_LED 3

HDD- 2

SLED 4

RESET- 5

PWSW+ 6

R758 100R/4

PWRBTIN (28,42)

RESET+ 7

PWSW- 8

NC

H2X510JM

**N31-2051331-H06**

For EMI

PWR\_LED

C691 X\_C0.1u16X/4

SUS\_LED

C710 X\_C0.1u16X/4

VCC3

R747 5.1K1%/4

SATA\_LED# (6,15)

R723 5.1K1%/4

Q111 NN-CMKT3904

IDE\_LED

VCC3

R725 5.1K1%/4

M.2\_1\_DAS (25)

R752 5.1K1%/4

Q113 NN-CMKT3904

IDE\_LED

VCC3

R739 5.1K1%/4

M.2\_2\_DAS (26)

R724 5.1K1%/4

Q112 NN-CMKT3904

IDE\_LED

VCC3

R717 5.1K1%/4

ASM1061\_HD\_LED# (23)

R705 5.1K1%/4

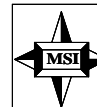
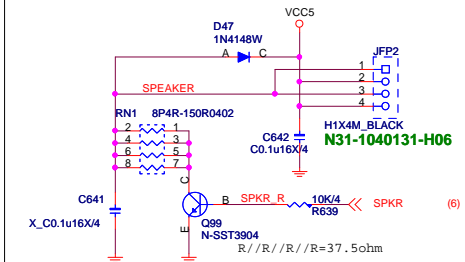
Q108 NN-CMKT3904

IDE\_LED

ASM HDLED#

Chip	Pin	Signal
VCCP_NB0	1	VCCP_NB1
CPU_VDDP0	1	CPU_VDDP1
VCC_DDR0	1	VCC_DDR1
CPU_1P80	1	CPU_1P8_1
CHIP_SOC0	1	CHIP_SOC1
CHIP_CLDO0	1	CHIP_CLDO1
VTT_DDR0	1	VTT_DDR1
VPP20	1	VPP1
CHIP_SOC_S50	1	CHIP_SOC_S5
CPU_1P8_S50	1	CPU_1P8_S5
CPU_VDDP_S50	1	CPU_VDDP_S5

Footprint:TESTPIN\_SMD30

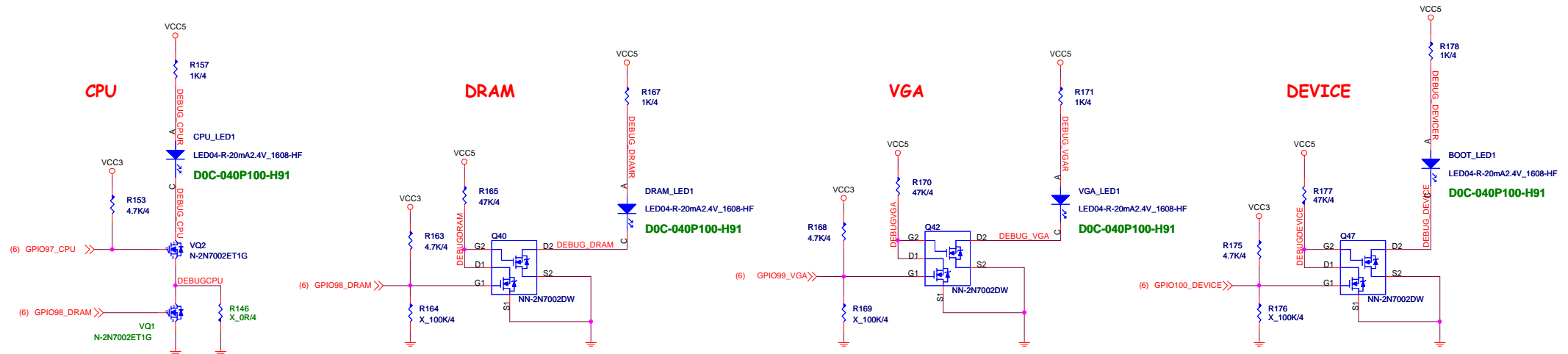


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3.0

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## EZ Debug LED



LED亮燈時同時將CPU LED關掉

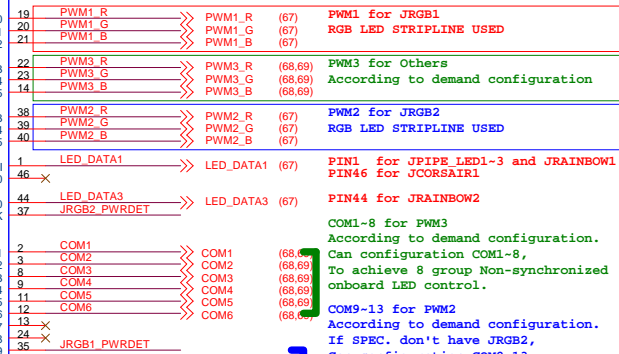
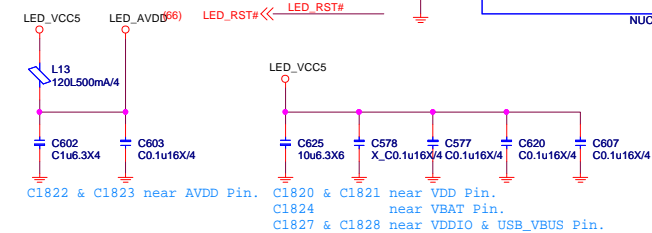
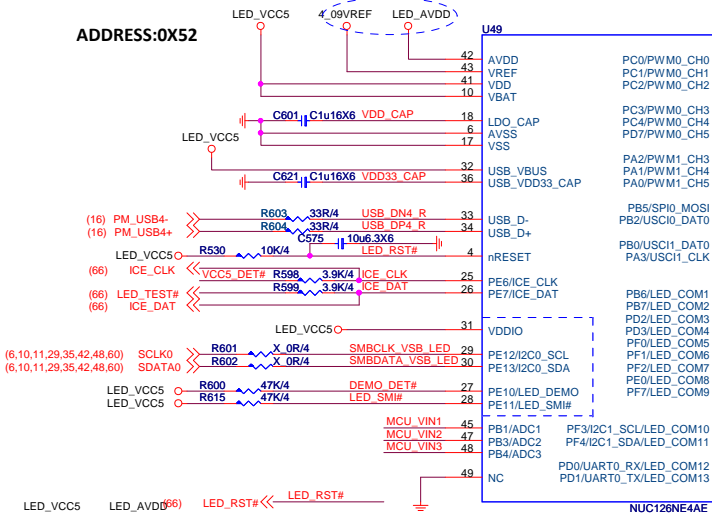
LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

## AMD AMP Detect LED

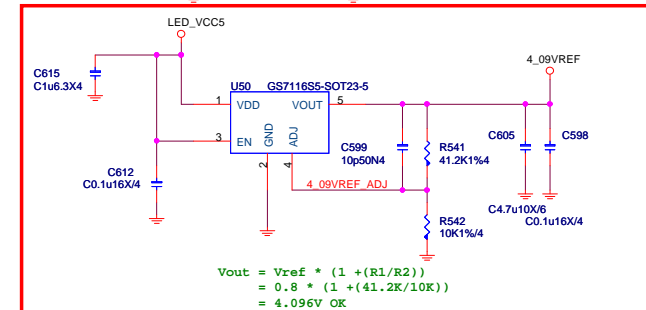
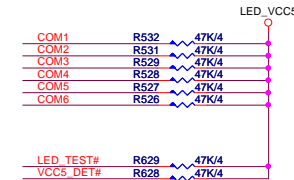
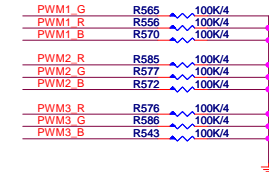


## 48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4\_09VREF stuff for VREF.

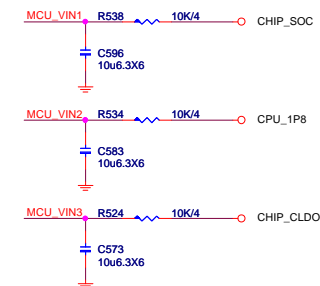


PS. COM1 is the first action block,  
next is COM2, and so on.  
Pin15,16 can configure to master  
smbus if spec requirement.



Option Spec For Voltage Monitor Require.

Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-13	PWM2

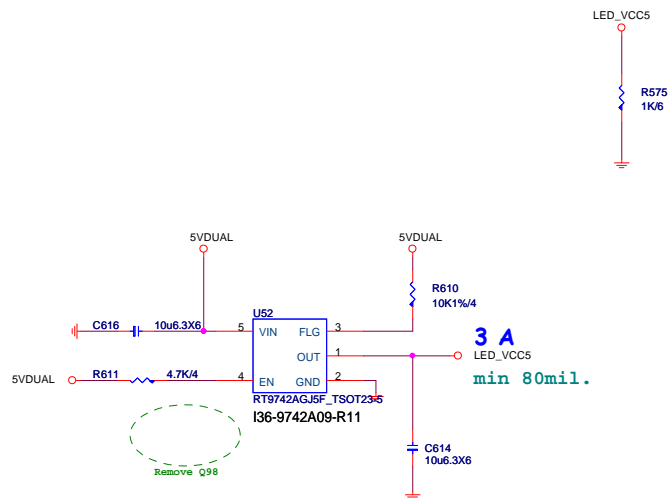


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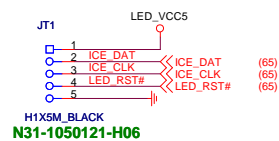
Size Custom	Document Description <b>MCU - LED Control</b>	Rev 3.0
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## EXTERNAL POWER INPUT



## External Power

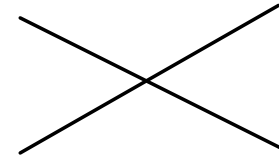
### JT1 for FW update



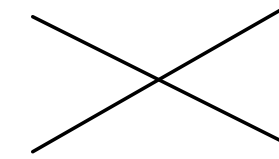
### JF1 For Factory Test



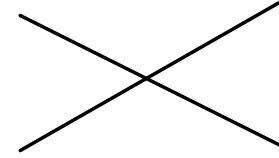
### 1 PCH HEATSINK LED



### 2 AUDIO/IO Cover LED



### 3 MOS HEATSINK LED



JPIPE:PIN1:output ,PIN2:input  
PIN2:MCU IN  
PIN1:HEATSINK OUT

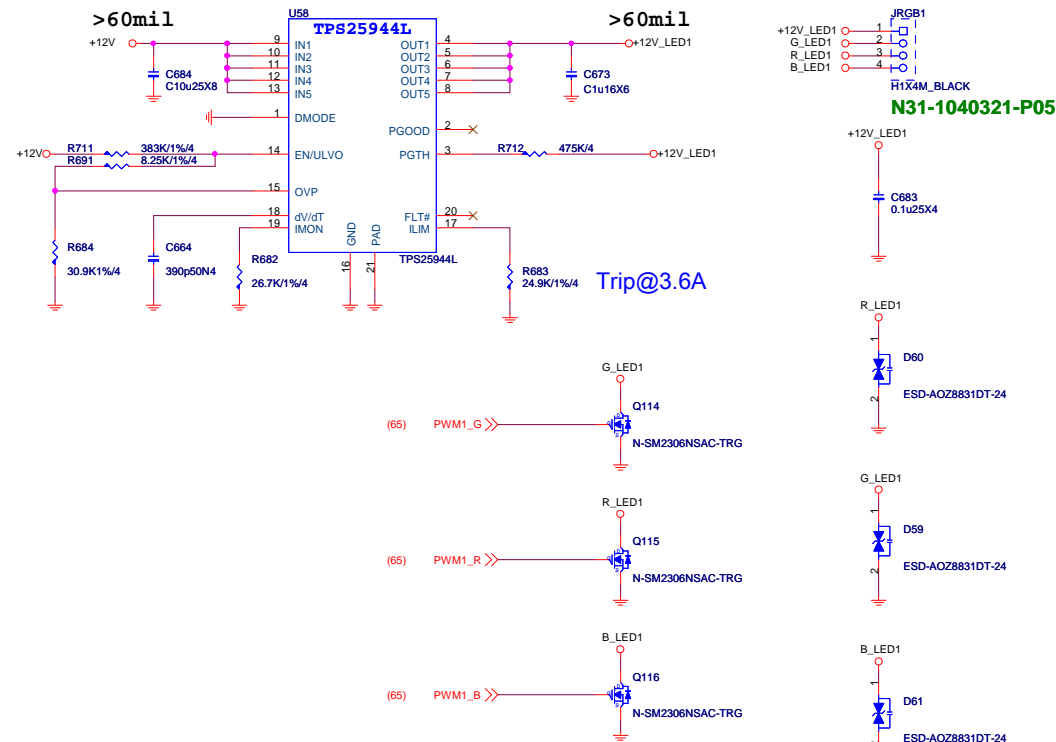


MICRO-STAR INT'L CO.,LTD

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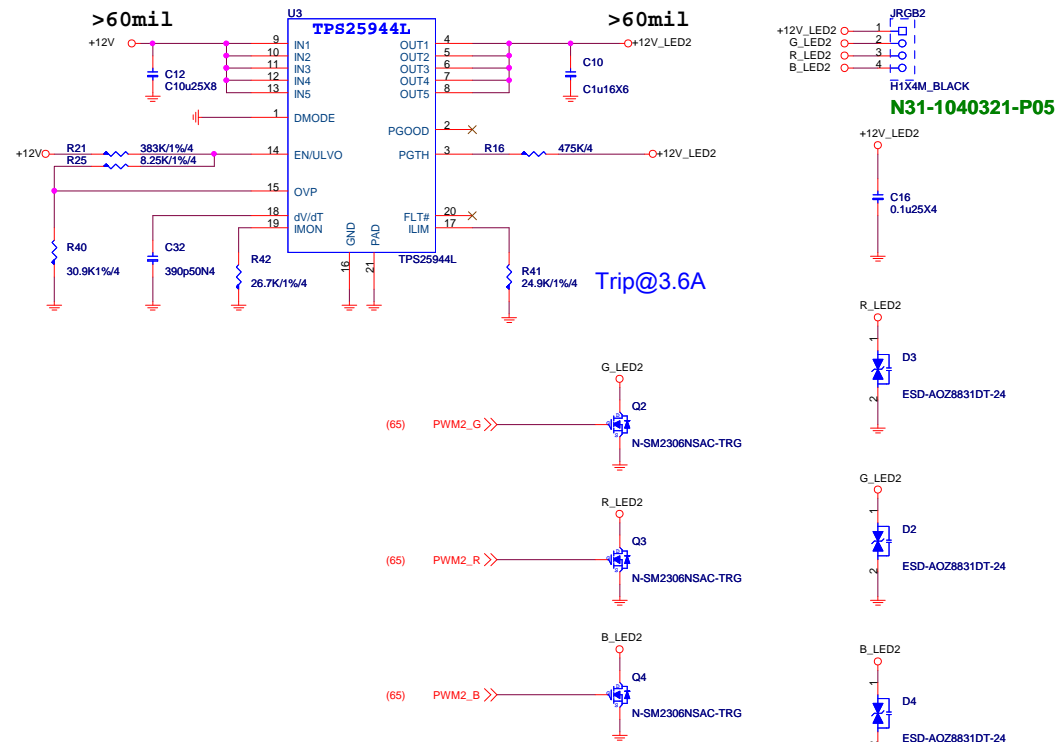
Size	Document Description	Rev
Custom	LED - Power / JPIPE	3.0
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## JRGB1



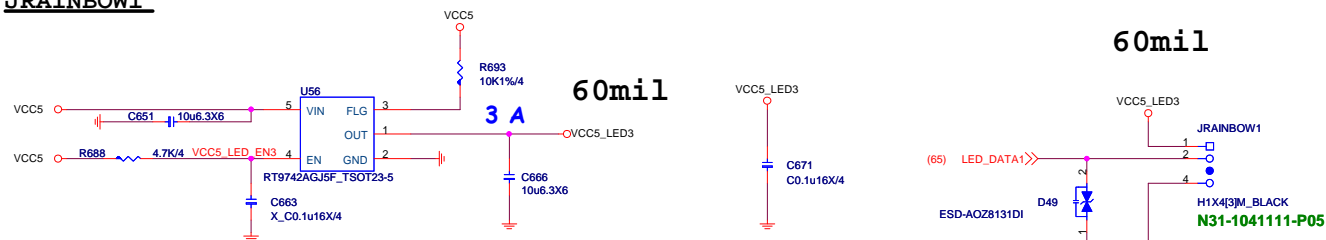
外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB1)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

## JRGB2

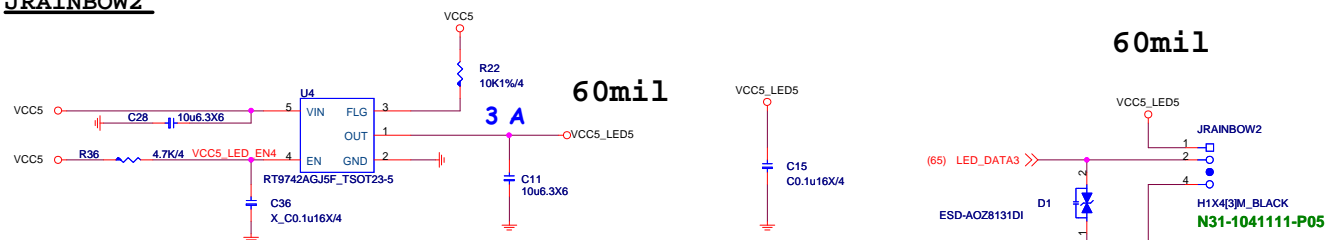


外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB2)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

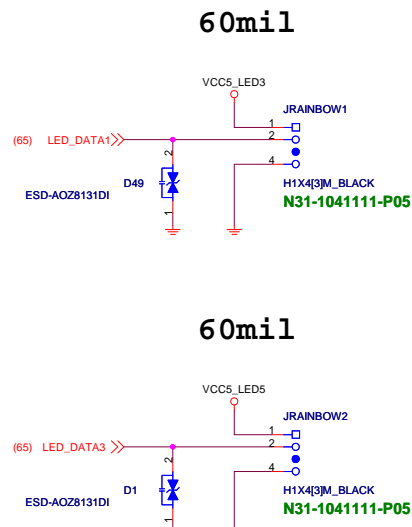
## JRAINBOW1



## JRAINBOW2

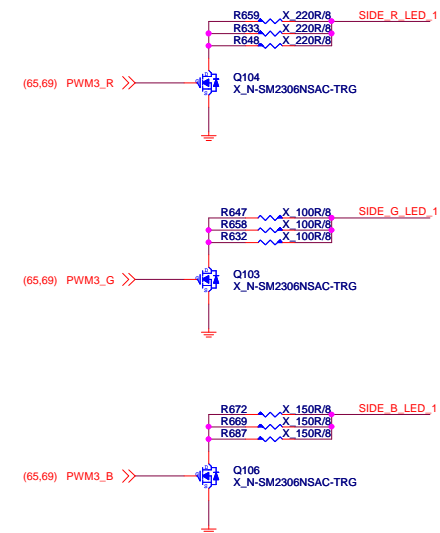
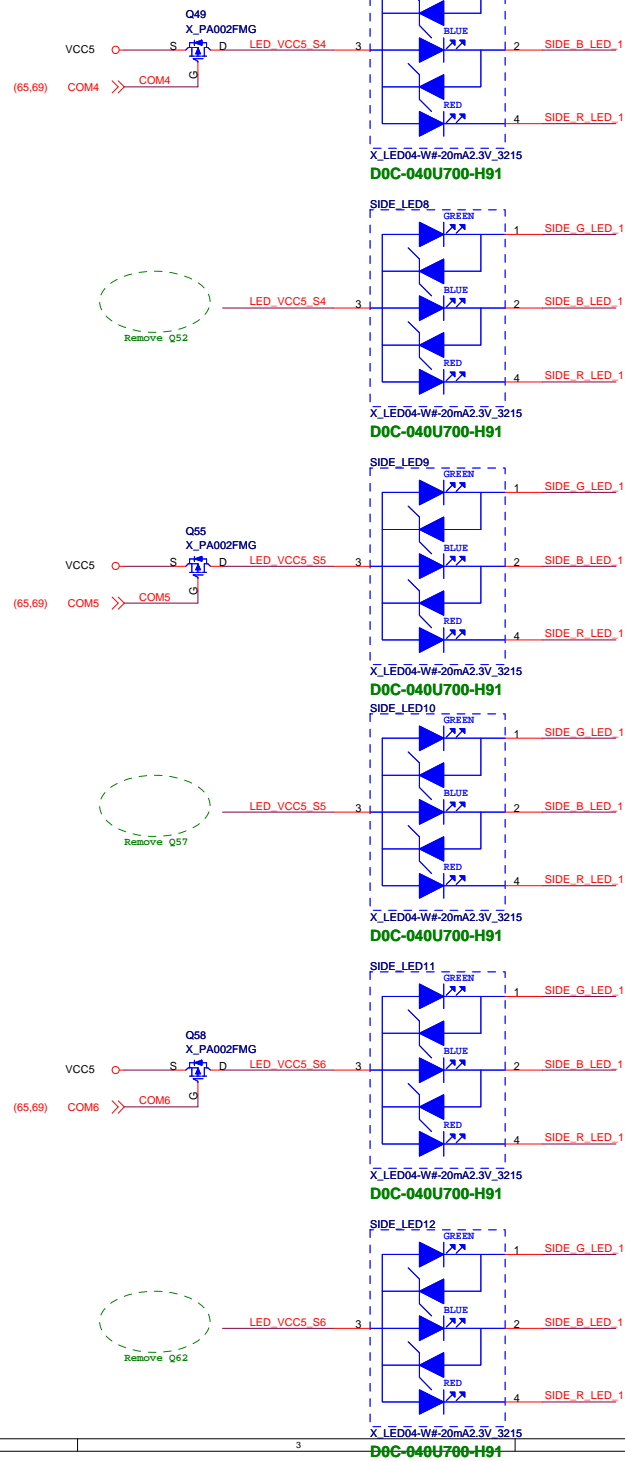
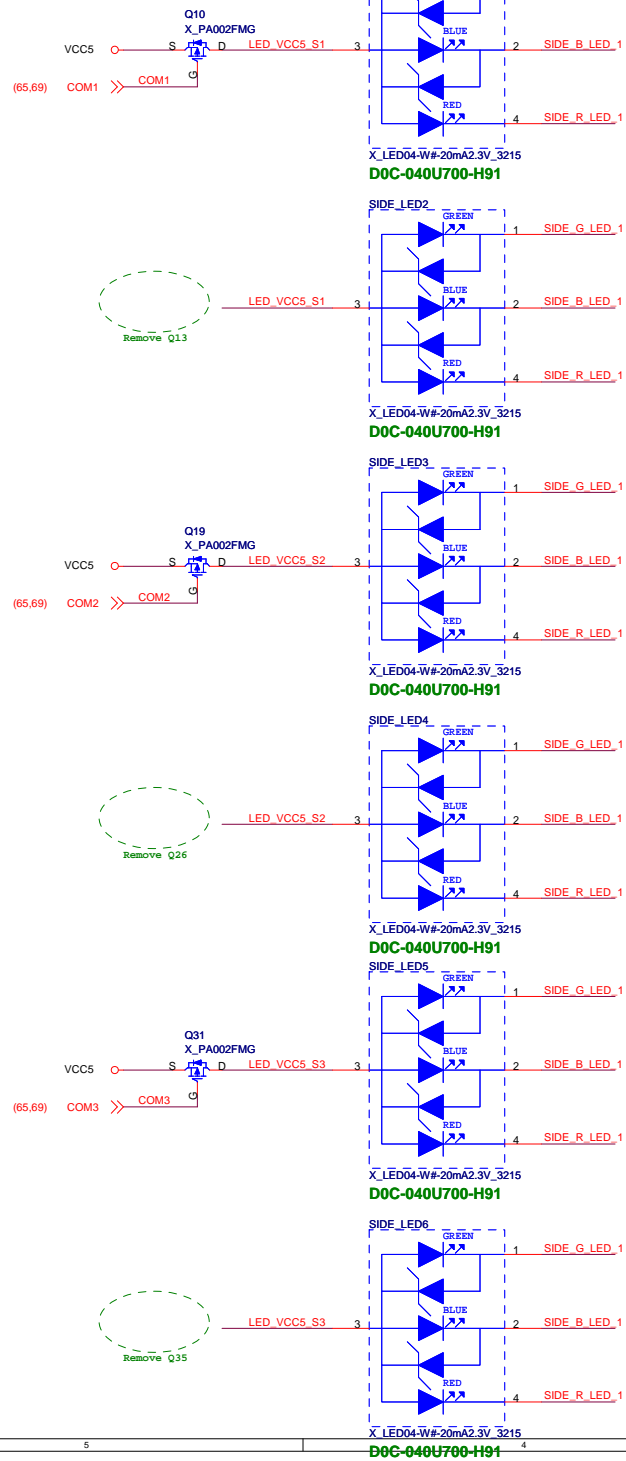


## JCORSAIR1



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Size	Document Description	Rev	
Custom	LED - JLED1 / 2 / 3 / 4	3.0	
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Sidebar LED \*12

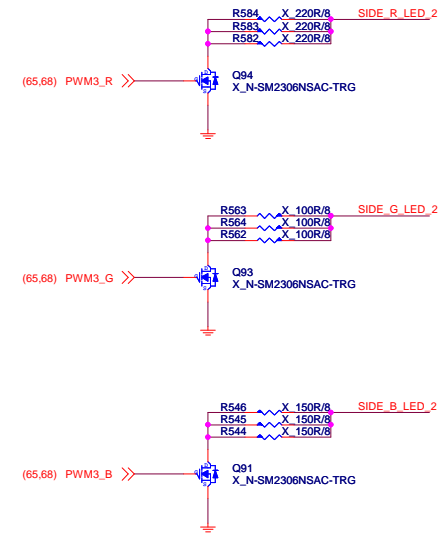
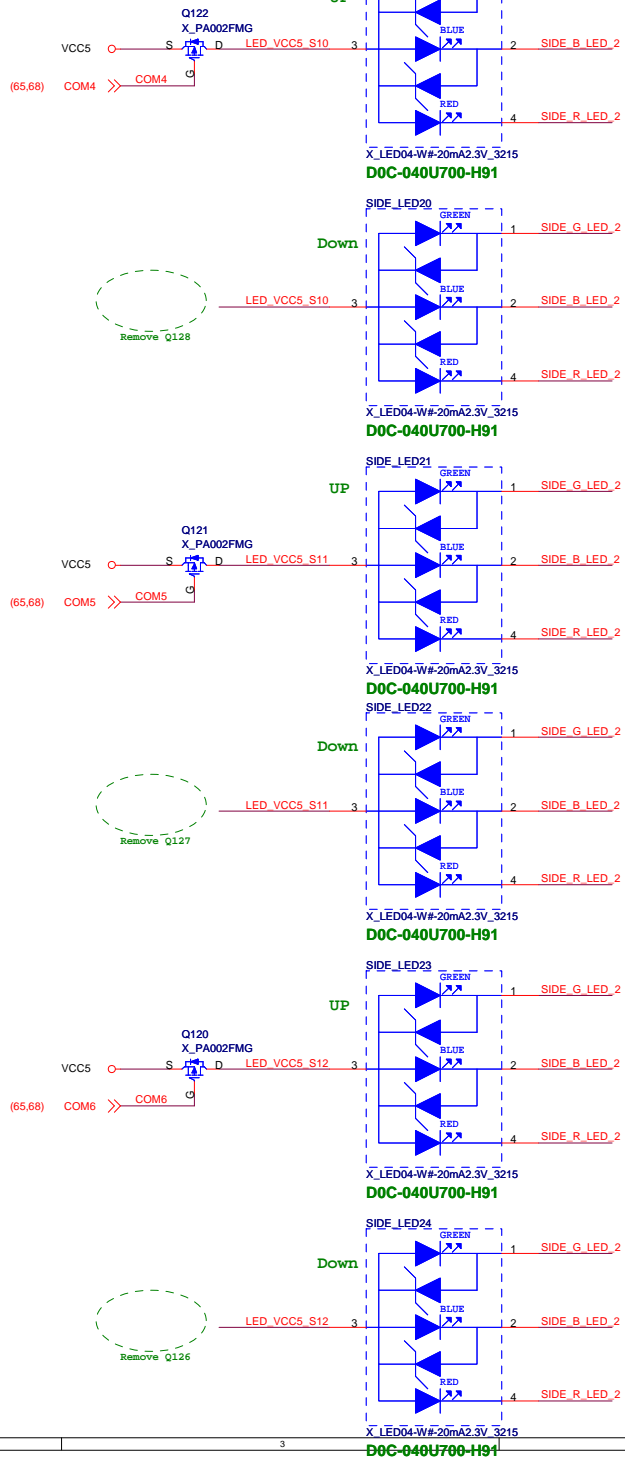
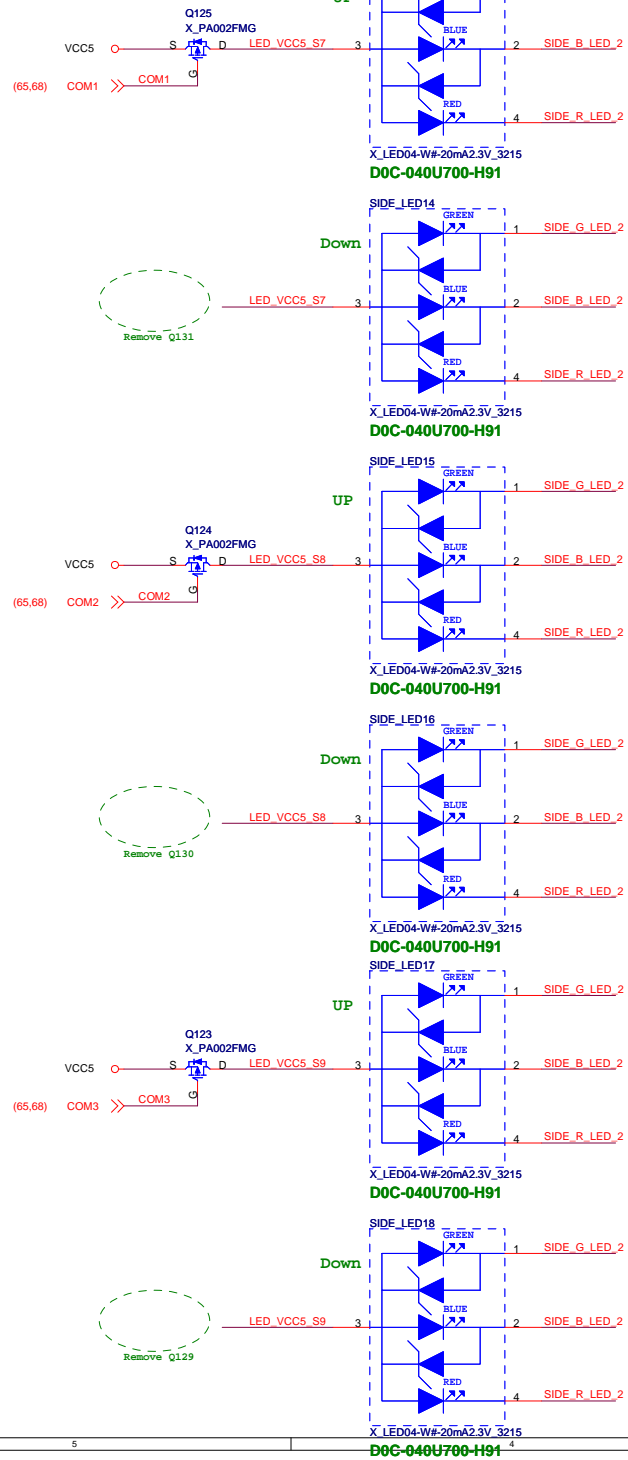


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MS-7C37

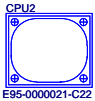
Size Custom	Document Description <b>LED - Sidebar LED</b>	Rev 3.0
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Market Name LED \*12



MSI			MICRO-STAR INT'L CO.,LTD	
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CPU Socket



E95-0000021-C22

PCB

PCB1

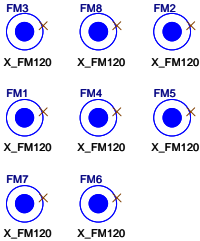
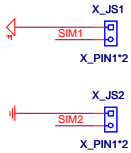


7C37-3.0  
PD0-07C3730-E48

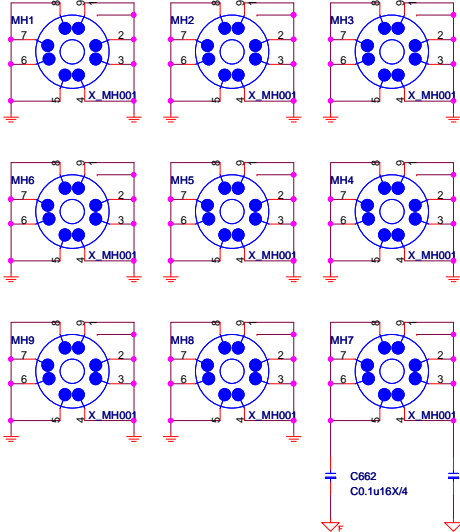
MOS HEATSINK

IO COVER

Simulation



Optics Orientation Holes



MANUAL PART

UEFI1  
G51-M1SPXXA-A09  
G51-M1SPXXA-A09

HDMI\_LA1  
Label  
HDMI  
HDMI LABEL  
Y01-RHDMI03-000

NAHIMIC1  
Y02-MU00100-NAH  
Y02-MU00100-NAH

XSPILT1  
X\_Y02-MA00401-XSP  
Y02-MA00401-XSP

SSE1  
X\_Y02-MA00101-SSE  
Y02-MA00101-SSE



AVZ1:  
D06-0100161-P52  
D06-0100101-X26

PCH HEATSINK

Audio COVER



DDR COVER